MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade, ISO 9001:2008 Certified)

Maisammaguda, Dhulapally, Secunderabad – 500100.

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

III B.TECH I SEMESTER

QUESTION BANK (2024-2025)

R15A0408

IC APPLICATIONS

R15

Code No: **R15A0408**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

IC Applications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART – A **(25 Marks)**

1. (a)What is virtual ground concept? Explain it. [2M]
   (b) List features of 723 Regulator [3M]
   (c) Draw the circuit diagram of all pass filter and write its output voltage equation.[2M]
   (d) List out the applications of 565 PLL. [3M]
   (e) Draw the circuit diagram of Weighted Resistor DAC. [2M]
   (f) List Specifications of ADC. [3M]
   (g) Write the difference between combinational and sequential circuits. [2M]
   (h) Draw the pin diagram of 8×1 Multiplexer. [3M]
   (i) How to convert the J-K flip flop to T flip flop. [2M]
   (j) Differentiate SRAM and DRAM. [3M]

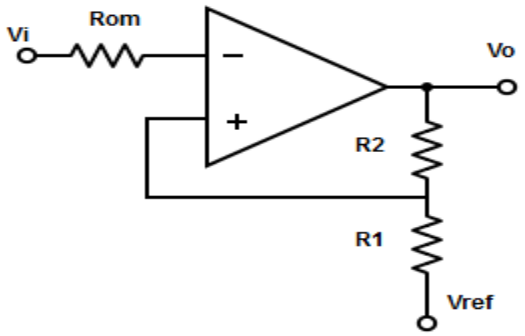
PART – B **(50 Marks)**

SECTION-I

2. a) Explain the operation of non-inverting Op-amp and derive the expression for output voltage? [8M]
   b) If the differential voltage gain and common mode voltage gain of a differential amplifier are 48dB and 2 dB respectively then calculate the CMRR. [2M]

(OR)

3. a)Explain the Working of Instrumentation Amplifier with suitable diagram. [5M]
   b) Calculate the hysteresis voltage for the schmitt trigger from the given specification: R_2 =56kΩ , R_1 = 100Ω , V_{ref} = 0v & V_{sat} = ±14v. [5M]



SECTION-II

4. a) Draw the circuit and explain the operation of 1st order LPF Butterworth filter. [5M]
   b) Design a wide band reject filter having f_H= 400 Hz and f_L= 2KHz with a pass band gain of 2. [5M]

(OR)

5. a) Draw the block diagram of Astable multivibrator operations using IC 555 and derive its time constant. [8M]
   b) Write the applications of PLL 565.[2M]

SECTION-III

6. Explain the operation of successive approximation ADC and discuss its merits and de-merits. [10M]

(OR)

7. Explain the R-2R ladder DAC and Inverted R-2R DAC with neat diagram.[10M]

SECTION-IV

8. Design binary to Gray code converter using gates.[10M]

(OR)

9. Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74×139 decoder .[10M]

SECTION-V

10. Explain Decade Binary Counter. [10M]

(OR)

11. a) Explain the functional behavior of Static RAM cell? Show the internal structure of 8X4 static RAM. [7M]
    b) List out the applications of ROM. [3M]

R15

Code No: **R15A0408**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations, November 2017

IC Applications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

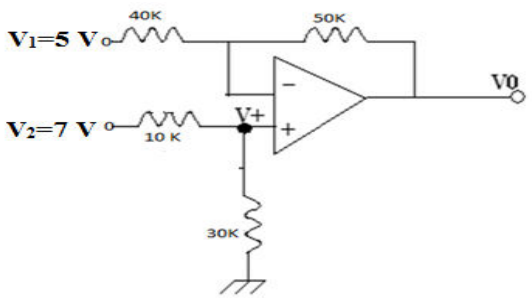
PART – A (25 Marks)

1. (a) Define slew rate [2]
(b) List out any 4 features of an instrumentation amplifier [3]
(c) Draw the pin diagram of 555 timer [2]
(d) Draw the internal block diagram of a 555 timer [3]
(e) Draw the circuit diagram of flash ADC [2]
(f) Compare the merits and demerits of various ADCs [2]
(g) Write the difference between combinational and sequential circuits [3]
(h) Explain briefly about Priority encoder [2]
(i) Draw the diagram of ROM architecture [3]
(j) Draw the circuit diagram of a S-R FF with JK FF [2]

PART – B (50 Marks)

SECTION – I

2. (a) Using IC7812, design a circuit to generate +5V output. [5]
(b) An adder-subtractor circuit designed using operational amplifier is shown below. Determine the output voltage for the given combinations of the inputs. Assume ideal op-amp. [5]



(OR)

3. (a) Define the term CMRR, Input offset voltage, input offset current, input bias current, out offset voltage with reference to OPAMPs. [5]
(b) Explain the operation of Schmitt trigger with the help of neat sketches. [5]

SECTION – II

4. (a) Design first order Butterworth low pass filter with high cutoff frequency $\mathbf{f_H}$ = 1.59 KHz and pass band gain of 10. Compute the gain at cutoff frequency. Plot the frequency response of the designed filter. [5]

   (b) Compare and contrast, minimum any four features of active filters with passive filters. [5]

OR

5. (a) Explain mono-stable multi vibrator using IC 555 [5]

   (b) If R_A = 6.8 K, R_B = 3.3 K, C = 0.1 μF in a 555 based astable multivibrator, calculate the following [5] 1) t_{high} 2) t_{low} 3) Free running frequency 4) Duty cycle

SECTION – III

6. (a) For a Digital to Analog converter (DAC) with 0-10 Volts range, calculate the values of LSB, MSB and output voltage for a digital input of 1010. Estimate the DAC's Quantization error. [5]

   b) Design a R-2R network for DAC [5]

(OR)

7. (a) Explain Successive approximation ADC with conversion process [5]

   (b) Explain dual slope ADC with neat diagram [5]

SECTION – IV

8. (a)Draw the 4 bit Parallel Adder (74LS283) and logic diagram. Explain its functioning with one example. [5]

   (b) What are decoders? Draw the pin diagram of and logic diagram of 4X16 Decoder (74HC154). [5]

(OR)

9. (a) Design binary to Gray code converter . [7]
   (b) Explain MUX [3]

SECTION – V

10. Design a Modulo-10 counter using any flip flop. [10]

(OR)

11. Design a conversion circuit to convert an S-R Flip Flop to J-K Flip Flop? [10]

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Code No: 115EB **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, March - 2017

LINEAR AND DIGITAL IC APPLICATIONS

(Common to BME, ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Show the standard representation of IC voltage regulator. [2]
b) Explain the precautions that can be taken to minimize the effect of noise on an OP-AMP circuit. [3]
c) Define stable and quasi stable state. [2]
d) Draw the circuit diagram of Second order high pass filter and give its transfer function. [3]
e) List out different types of A/D converters. [2]
f) What do you mean by quantization error in an A/D converter? [3]
g) Give the working principle of analog multiplexer. [2]
h) How to interface the TTL logic gates to the CMOS logic? [3]
i) What is meant by state diagram? [2]
j) Write the specifications of counter IC's. [3]

PART - B

(50 Marks)

2. Design a differentiator circuit that will differentiate input signal with f_{max} = 100Hz. [10]

OR

3.a) What are the differences between the inverting and non inverting terminals? What do you mean by the term "virtual ground"?
b) Explain the method of boosting the current of a three terminal voltage regulator. [5+5]

4. Design and explain the operation of All Pass Filter with its characteristics. [10]

OR

5.a) Draw the circuit of Schmitt trigger using 555 timer and explain its operation.
b) Draw the circuit of a PLL AM detector and explain its operation. [5+5]

6. Draw the schematic block diagram of Dual-slope A/D converter and explain its operation. Derive expression for its output voltage V_o. [10]

OR

7.a) What is the conversion time of a 10 bit successive approximation ADC if its input clock is 5 MHz?
b) List the specifications of DAC. [5+5]

8.a) Design a 5 to 32 line decoder using 3 to 8 line decoder, active low outputs with 2 active low and one active high enable.

b) What do you mean by Carry propagation delay? Design a 4-bit Carry look ahead generation circuit? [5+5]

OR

9. Draw and explain the block diagram of n-bit parallel binary adder/subtractor. [10]

10.a) Explain operation of DRAM cell array.

b) Design and implement FIFO shift register using IC's. [5+5]

OR

11.a) Design and implement 4-bit synchronous down counter using IC.

b) Explain the internal structure of ROM. [5+5]

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R13

Code No: 115EB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, November/December - 2016

LINEAR AND DIGITAL IC APPLICATIONS

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define unity gain band width of an op-amp. [2]
b) Define slew rate. What causes it? [3]
c) What is switched capacitor filter? [2]
d) Draw the circuit diagram of AM detector using PLL. [3]
e) Which type of ADC is the fastest? Why? [2]
f) An 8 bit DAC has a resolution of 20mv/bit. What is analog output voltage? [3]
g) Mention any two applications of multiplier IC. [2]
h) Realize EX-OR gate with CMOS circuit. [3]
i) Write the difference between static and dynamic RAM's. [2]
j) Draw the block diagram of 3-bit ring counter. [3]

PART - B

(50 Marks)

2. With neat circuit diagram explain the operation of Schmitt trigger. [10]

OR

3.a) An IC op-amp 741 used as an inverting amplifier with a gain of 100. The voltage gain vs frequency characteristic is flat up to 12 kHz. Find the maximum peak to peak input signal that can be feed without causing any distortion to the output.
b) Draw and explain the output waveform of the ideal inverter circuit when the input is square wave. [5+5]

4. Explain the operation of mono stable multi vibrator using 555 timers. Derive the expression of time delay of mono stable multi vibrator with 555 timers. [10]

OR

5.a) From the given component values find the free running frequency. Control voltage Vc=10.9v, Vcc=12v, R1=4.7k and C1=1.1Nf.
b) Design a narrow band bandpass filter using op-amp. The resonant frequency is 100HZ and Q=2. Assume c=0.1Uf. [5+5]

6. Draw the schematic block diagram of dual slop A/D converter and explain its operation. Derive expression for its output voltage. [10]

OR

7.a) What are the limitations of weighted resistor type D/A converter?
b) What do you mean by quantization error in an A/D converter? [5+5]

8. Find the state diagram and state table of a binary coded decimal to excess-3 decoder. [10]

OR

9. Draw the basic DTL gate and explain its operation. [10]

10.a) Design a 4 to 16 decoder using two 74×138 IC's.
b) Implement the following Boolean expression using 74×151 IC F(z)=AB+BC+AC. [5+5]

OR

11. With the help of timing diagram explain read and write operations of SRAM. [10]

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Code No: 115EB

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech III Year I Semester Examinations, November - 2015
LINEAR AND DIGITAL IC APPLICATIONS
(Common to ECE, BME)

COLLEGE OF ENGG. & TECH. LIBRARY SECUNDERABAD

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A (25 Marks)

1.a) Significance and definition of upper and lower threshold points of a Schmitt trigger. [2]
b) Mention the reasons why open loop is not preferred for linear applications. [3]
c) List various applications of IC 555 Timer. [2]
d) Differentiate Bessel, Butterworth and Chebyshev filters. [3]
e) Define the following terms as related to DAC: i) Linearity ii) Resolution. [2]
f) Compare R-2R and Weight Resistor types of ADC. [3]
g) What is meant by Tri-state logic? [2]
h) What is the purpose of priority encoders. [3]
i) Write the applications of shift registers. [2]
j) Differentiate Static and Dynamic RAMs. [3]

PART - B (50 Marks)

2.a) Explain the why emitter follower circuit is used as level shifter.
b) Design an op-amp differentiator to differentiate an input signal that varies in frequency from 10Hz to about 1 KHz. [5+5]

OR

3.a) What are the disadvantages of using zero crossing detector? How it can be overcome using Schmitt trigger?
b) Draw the internal architecture of IC 723 voltage regulator and explain. [5+5]

4.a) Draw the block diagram for PLL and explain in detail.
b) Explain two of the following applications for which PLL is used:
i) AM detector ii) FM demodulator. [4+6]

OR

5.a) An ideal low pass filter having f_H=5 kHz is cascaded with high pass filter having f_L=4.8 kHz. Sketch the frequency response of the cascaded filter.
b) Explain the monostable operation of the 555 timer and derive the expression for the period of a pulse generated by the Timer. [5+5]

6.a) Explain the operation of the fastest analog to digital converter. What is the main draw back of this converter? Compare this converter with other types.
b) Draw the circuit of a Ladder type DAC for 4 bits and derive expression for output voltage. [5+5]

OR

7.a) Draw a schematic diagram of a D/A converter. Use resistance values whose ratios are multiples of 2. Explain the operation of the converter.
b) Give the schematic circuit of integrating type A/D converter and explain the operation of this system and derive expression for output voltage Vo. [5+5]

8.a) Draw the resistive model of a CMOS inverter and explain its behavior for LOW and HIGH outputs.

b) Design 1:8 demultiplexer using two 1:4 demultiplexer. [6+4]

OR

9.a) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how?

b) Design a full subtractor with NAND gates. [5+5]

10.a) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the above shift register with the help of timing waveforms.

b) Explain the functional behavior of Static RAM cell? Show the internal structure of 8×4 static RAM. [5+5]

OR

11.a) Design a 4-bit binary synchronous counter using 74×74.

b) Draw the internal structure of synchronous SRAM and explain the operation. [5+5]

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N3

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING B.Tech III year – I Semester Examinations, Model Paper-1 Linear and Digital IC Applications

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1. a. What is virtual ground? (2 M)
   b. What are the characteristics of an Ideal op-amp? (3 M)
   c. What is an active filter? (2 M)
   d. Classify filters based on frequency range of operation (3 M)
   e. What are different types of DACs? (2M)
   f. What are the drawbacks of weighted resistor DAC? (3M)
   g. Classify the integrated circuits (2 M)
   h. Write short notes about code converters (3 M)
   i. What is a flip flop? (2 M)
   j. Write short notes on SR flip flop (3M)

PART-B (5*10=50 Marks)

2. Draw and explain the waveforms of inverting and non-inverting Comparator (10M)

OR

3. Explain the working of an ideal & practical differentiator (10M)

4 With a neat diagram explain about triangular wave generator and derive the frequency of Oscillation (10M)

OR

5 With a neat diagram explain about sawtooth wave form generator (10M)

6 Explain the operation of parallel comparator type ADC with the help of a neat diagram (10M)

OR

7 Explain the operation of a Successive approximation type analog to digital converter (10M)

8 Explain Binary to Gray and Gray to Binary code conversion with one example each (10M)

OR

9 Explain the IC interfacing between TTL and CMOS

10 Draw the D filp-flop and T flip-flop and explain the operation with truth table (10M)

OR

11. (a) Draw the JK flip-flop and explain it's operation with truth table (5M)
    (b) Explain D flip-flop with help of diagram and truth table (5M)

MRCET

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING B.Tech III year – I Semester Examinations, Model Paper-2 Linear and Digital IC Applications

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1. **a)** How many types of waveforms are generated with the use of a waveform generator (2M)
   b) Draw the waveforms that a waveform generator can generate (3M)
   c) What is a comparator (2M)
   d) Explain inverting comparator briefly (3M)
   e) What is Resolution (2M)
   f) Calculate the number of bits required to represent a full scale voltage Of 10V with a resolution of 5mV approximately (3M)
   g) Write short notes on BCD to Binary converter (2M)
   h) Explain briefly the magnitude comparator (3M)
   i) Write the truth table for J-K flip-flop (2M)
   j) Draw the serial and parallel shift register (3M)

MRCET

PART-B (5*10=50 Marks)

2 Draw and explain the operation of an op-amp as an integrator (10M)

OR

3 Explain the modes of operation of an op-amp (10M)

4 How a symmetrical wave form generator can be constructed using 555 timer (10M)

OR

5 If R_A = 6.8 KΩ, R_B = 3.3 KΩ, C = 0.1μF in 555 Astable Multivibrator. Calculate
i) t_{high} ii) t_{Low} iii) Free running frequency iv) Duty Cycle (10M)

6 a) Calculate the number of bits required to represent a full scale voltage of 10V with a Resolution of 5mV approximately (5M)
b) List out different types of A/D converters (5M)

OR

7 Explain the operation of weighted resistor DAC with neat circuit diagram (10M)

8 a) Explain 4 bit parallel adder (5M)

b) Explain 4-bit magnitude comparator (5M)

OR

9 Explain Decoders (10M)

10 Explain 3 bit asynchronous counter with neat diagram (10M)

OR

11 a) Assume the propagation delay of each flip-flop is 12 ns. What is the total propagation delay and the max clock frequency of a 3 bit asynchronous Binary counter (5M)

b) Explain the 2-bit synchronous binary counter (5M)

MRCET

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING B.Tech III year – I Semester Examinations, Model Paper-3 Linear and Digital IC Applications

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1	a) What is a voltage regulator	(2M)
	b) Mention the features of 723 regulators	(3M)
	c) What is IC 555 timer	(2M)
	d) Draw the functional diagram of IC 555 timer	(3M)
	e) What is the disadvantage of Weighted resistor DAC	(2M)
	f) Draw the circuit diagram of DAC which overcome the disadvantage of Weighted resistor DAC	(3M)
	g) Mention the classification of Integrated Circuits	(2M)
	h) Write comparison of various logic families	(3M)
	i) What is a decoder	(2M)
	j) Write short notes on Parallel binary adder	(3M)

PART-B (5*10=50 Marks)

2 Explain inverting & non-inverting comparator (10M)

OR

3 a)Explain the Schmitt trigger (5M)

b) Explain the features of 723 regulators (5M)

4 Draw and explain the frequency response of all filters based on frequency range (10M)

OR

5 a) Write the design steps for 1st order LPF (5M)

b) Explain the frequency scaling (5M)

6 Explain about ladder type DAC with neat diagram (10M)

OR

7 What is the drawback of weighted resistor DAC. Write down the method to Overcome this drawback (10M)

8 Explain Encoders (10M)

OR

9 Explain an 8-input Data Selector / Multiplexer (10M)

MRCET

10 Explain the synchronous BCD decade counter (10M)

OR

11 What is the shift register? Explain different kinds of shift register (10M)

MRCET

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-4

Linear and Digital IC Applications

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1	a) How many modes of operation of op-amp are there?	(2M)
	b) Name the operation modes of op-amp.	(3M)
	c) Draw the frequency response of Band pass & Band reject filters	(2M)
	d) Draw the circuit of 1^{st} order LPF	(3M)
	e) Mention various types of DACs	(2M)
	f) Draw the circuit diagram of weighted resistor DAC	(3M)
	g) Write classification of Integrated circuits	(2M)
	h) Write comparison of ECL, TTL and CMOS families	(3M)
	i) What is a flip-flop?	(2M)
	j) Explain briefly about the S-R flip-flop	(3M)

PART-B (5*10=50 Marks)

2	Explain three terminal voltage regulators	(10M)
	OR	
3	Explain the inverting and non-inverting AC amplifier	(10M)
4	Explain the functional diagram of IC 555 timer	(10M)
	OR	
5	Explain the monostable multivibrator operation and derive it's pulse width	(10M)
6	Explain the DAC and ADC specifications.	(10M)
	OR	
7	Explain the counter type ADC	(10M)
8	a) Explain 4 line to 16 line demultiplexer	(5M)
	b) Explain parity generators/checkers	(5M)
	OR	
9	Use 74HC85 comparators to compare magnitudes of two 16 bit numbers. Show the comparators with proper interconnections	(10M)

MRCET

10	Explain asynchronous Decade counters	(10M)
	OR	
11	Explain ROM and it's types and RAM and it's types	(10M)

MRCET

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING B.Tech III year – I Semester Examinations, Model Paper-5 Linear and Digital IC Applications

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1	a) What is a differentiator	(2M)
	b) What is an Integrator	(3M)
	c) What is all-pass filter	(2M)
	d) Draw the circuit diagram of HPF	(3M)
	e) Draw the circuit diagram of R-2R ladder DAC	(2M)
	f) Mention different types of ADC	(3M)
	g) Write comparison of various logic families	(2M)
	h) Write about Gray to binary convertor	(3M)
	i) Mention the types of counter	(2M)
	j) What is a shift register?	(3M)

PART B

2 Prove that the difference amplifier with unity gain is a subtractor (10M)

OR

3 Explain DC and AC characteristics of op-amp (10M)

4 Explain the Astable multivibrator and derive it's frequency operation (10M)

OR

5 Draw and explain block schematic of PLL (10M)

6 Explain the DAC & ADC specifications (10M)

OR

7 Explain the Dual slope ADC (10M)

8 Explain half adder and full adder with an example each (10M)

OR

9 a) Explain the decimal-to-BCD priority encoder (5M)

b) Explain BCD-to-Binary conversion (5M)

10 What is a flip-flop? Explain SR, D and JK flip-flops (10M)

OR

11 Explain various kinds of shift registers (10M)

MRCET

R15A0409

ANALOG COMMUNICATIONS

R15

Code No: **R15A0409**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

Analog Communications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART – A (25 Marks)

1. (a) What is the bandwidth required for an amplitude modulated signal?[2M]
   (b) What is the need for modulation in communication systems? [3M]
   (c) What are the advantages of SSBSC over DSBSC, AM? [2M]
   (d) What is Hilbert transform & what are its applications? [3M]
   (e) Define Carson's rule for bandwidth of FM systems? [2M]
   (f) Compare NBFM & WBFM [3M]
   (g) Give the mathematical representation of narrow band noise.[2M]
   (h) Compare the noise performance of FM and AM systems. [3M]
   (i) Draw the block diagram of FM receiver.[2M]
   (j) Compare PAM,PWM,PPM systems.[3M]

PART – B (50 Marks)

SECTION – I

2. a) Explain how an amplitude modulated signal can be detected using a square law detector.[6M]
   b) An AM transmitter radiates 50W power when carrier is modulated and μ=0.707. Determine i) carrier power ii) modulation efficiency [4M]

(OR)

3. a) Explain how a DSBSC signal is represented in the time and frequency domain,[5M]
   b) Explain how a DSBSC signal is generated using a balanced modulator.[5M]

SECTION – II

4. a) Explain how a SSBSC signal is generated using a filter method.[5M]
   b) Compare different amplitude modulation techniques. [5M]

(OR)

5. a) Explain the generation of VSBSC signal [5M]
   b) What are the applications of different amplitude modulation systems.[5M]

SECTION – III

6. a) Derive the expression for single tone frequency modulated signal.[5M]]
   b) A 100 M Hz carrier is frequency modulated by a sinusoidal signal of amplitude 20V and frequency 100K Hz .The frequency sensitivity of the modulator is 25K Hz/volt. Determine i) frequency deviation ii) modulation index (β) iii) bandwidth [5M]

(OR)

7. a) Explain about pre emphasis and de emphasis in FM systems [6M]
   b) Compare AM & FM [4M]

SECTION – IV

8. a)Define i) Noise bandwidth Ii) Noise figure [4M]
   b) Derive the expression of figure of merit for Amplitude modulated system.[6M]

(OR)

9. a) Derive the expression of figure of merit for DSBSC system.[5M]
   b) Derive the expression of figure of merit for frequency modulated system [5M]

SECTION – V

10. a) Explain the characteristics of a radio receiver.[4M]
    b) Explain the operation of Tuned radio frequency (TRF) receiver with the block diagram and mention its advantages and disadvantages. [6M]

(OR)

11. Explain the generation and de modulation of PAM signals.[10M]

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Code No: R15A0409

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations, November 2017

Analog Communications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

*****

PART – A (25 Marks)

1. (a) What is the maximum transmission efficiency of an amplitude modulated system for 100% modulation?[2M]
   (b) A carrier signal $c(t)= 20\cos(2\pi 10^6 t)$ is modulated by a message signal $m(t)= 5\cos(2\pi 10^4 t)$ to generate a DSBSC signal. Calculate bandwidth and power? [3M]
   (c) Compare AM, DSBSC and SSBSC? [2M]
   (d) What is Hilbert transform & what are its applications? [3M]
   (e) What is the relation between FM and PM? [2M]
   (f) Compare NBFM and AM. [3M]
   (g) Give the mathematical representation of narrow band noise. [2M]
   (h) Compare the noise performance of different AM systems. [3M]
   (i) Draw the block diagram of TRF receiver. [2M]
   (j) Compare PAM, PWM, PPM systems.[3M]

PART – B (50 Marks)

SECTION – I

2. a) Explain how an amplitude modulated signal can be generated using a switching modulator.[6M]
   b) Consider an AM signal $s(t)=20(1+0.9\cos 2\pi 10^4 t)\cos 2\pi 10^6 t$.The signal is radiated into free space using an antenna having resistance of 5Ω. Calculate i) Power ii) Bandwidth iii) modulation efficiency [4M]

(OR)

3. a) Explain how a DSBSC signal is represented in the time and frequency domain,[5M]
   b) Explain how a DSBSC signal is detected using a coherent detector.[5M]

SECTION – II

4. a) Explain how a SSBSC signal is represented in time and frequency domain.[5M]
   b) Explain how a SSBSC signal is generated using phase shift method. [5M]

(OR)

5. a) Explain the detection of VSBSC signal [5M]
   b) What are the applications of different amplitude modulation systems. [5M]

SECTION – III

6. a) Derive the expression for Narrow band frequency modulated signal.[5M]]
   b) Consider an FM signal $s(t)=10\cos(2\pi\ 10^6t+8\sin 4\pi\ 10^3t)$.Determine i)Modulation index ii) frequency deviation iii) power iv) bandwidth [5M]

(OR)

7. a) Explain how a frequency modulated signal is generated using varactor diode [5M]
   b) Explain how a FM signal is demodulated using PLL(Phase locked loop) [5M]

SECTION – IV

8. a)Define i) Noise bandwidth ii) Noise figure [4M]
   b) Derive the expression of figure of merit for Frequency modulated system. [6M]

(OR)

9. a) Derive the expression of figure of merit for SSBSC system.[6M]
   b) Explain about the noise temperature. [4M]

SECTION – V

10. a) Explain the characteristics of a radio receiver.[4M]
    b) Explain the operation of super hetero dyne receiver with the block diagram and mention its advantages and disadvantages. [6M]

(OR)

11. Explain the generation and demodulation of PPM signals.[10M]

*****

Code No: 115AK **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, March - 2017

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Write the expression for amplitude modulated wave. [2]
b) What are the methods for detecting AM waves? [3]
c) Draw the frequency domain representation of SSB modulated wave. [2]
d) Compare different AM techniques. [3]
e) Define modulation index for FM. [2]
f) Differentiate FM and AM. [3]
g) What are the different types of noise sources in analog communication? [2]
h) How do you define the effective noise temperature? [3]
i) What are image frequencies? Explain. [2]
j) What is the need for AGC circuit? [3]

PART - B

(50 Marks)

2.a) Derive the relation between the output power of an AM transmission and the depth of modulation.
b) When the modulation percentage is 75, an AM transmitter produces 10KW. How much of this is carrier power. What would be the percentage power saving if the carrier and one of the side bands were suppressed? [5+5]

OR

3.a) Draw the circuit diagram for balanced ring modulator and explain its operation indicating all the waveforms of the modulator.
b) What is the effect of frequency and phase error in demodulation of DSB-SC wave using synchronous detector. [5+5]

4.a) Discuss various methods used to generate SSB signals with neat sketches.
b) Explain the need of VSB modulation. [5+5]

OR

5. Describe the time domain band-pass representation of VSB. Draw and explain the block diagram of VSB generation corresponding to the time domain description. [10]

6.a) Derive the expression for FM signal from fundamentals and differentiate narrow band FM and wide band FM.

b) Explain the principle of direct method of generation of FM signal using relevant diagrams. [5+5]

OR

7. Prove that narrow band FM offers no improvement in SNR over AM. [10]

8.a) Derive the equation for noise figure of FM receiver.

b) What is the purpose of pre-emphasis and de-emphasis filtering? Explain the filtering process with suitable sketches. [5+5]

OR

9. Compare noise performance of PM and FM system. [10]

10.a) Explain the working of tuned radio frequency receiver with the help of a block diagram.

b) Give the comparison between phase discriminator and ratio detector. [5+5]

OR

11.a) Explain with a neat block diagram PPM generation and detection.

b) Write short notes on time division multiplexing. [5+5]

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Code No: 115AK **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year I Semester Examinations, November/December - 2016

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define noise. [2]

b) What are the similarities and differences between narrowband FM and AM systems? [3]

c) What is threshold effect in envelope detector? [2]

d) Distinguish between simple AGC and delayed AGC. [3]

e) Define the terms frequency deviation and modulation index for FM wave. [2]

f) Explain the need for modulation. [3]

g) Give the classification of radio transmitters. [2]

h) Explain the need of amplitude limiter in FM receiver. [3]

i) Calculate the percentage saving in power if only one side band transmission is used over the DSB-SC system at (i) 100% modulation (ii) 50% modulation. [2]

j) State the sampling theorem. [3]

PART - B

(50 Marks)

2.a) Define modulation and explain the need of modulation.

b) A carrier with amplitude modulated to a depth of 50% by a sinusoidal, produces side band frequencies of 5.005 MHz and 4.995MHz. The amplitude of each side frequency is 40V. Find the frequency and amplitude of the carrier signal. [5+5]

OR

3.a) Draw the block diagram and explain generation of DSB-SC signal using balanced modulator.

b) A modulating signal is a multi-tone signal given by
$m(t) = A_1 \cos w_1 t + A_2 \cos w_2 t + A_3 \cos w_3 t$.
The signal m (t) modulates a carrier Ac $\cos w_c t$. Plot the signal sided spectrum and find the bandwidth of the modulating signal. Assume that $w_3 > w_2 > w_3$ and $A_3 > A_2 > A_1$. [5+5]

4.a) What is SSB Modulation and what are its advantages? Draw the block diagram for SSB generation using Phase discrimination method and explain its operation.

b) Explain how the base band signal can be recovered from the VSB Signal plus carrier using envelope detector. [5+5]

OR

5.a) Mention applications of different AM Systems.

b) A vestigial filter has a transfer function H (f) with $f_c = 10^5$Hz. Find the VSB modulated signal when $e_m(t) = \cos(2\pi f_m t)$ and $e_c(t) = 2\cos(2\pi f_c t)$. Assume $f_m = 10^3$Hz. [5+5]

6.a) Discuss the effect of modulation index on the band width of FM. Explain the generation of WBFM from NBFM with neat sketch.

b) A carrier is frequency modulated by a sinusoidal modulating of frequency 2 kHz, resulting in a frequency deviation of 5 kHz. What is the bandwidth occupied by the modulated waveform? The amplitude of the modulating sinusoid is increased by a factor 2 and its frequency lowered by 500Hz. What is the new bandwidth? [5+5]

OR

7.a) Compare the direct and indirect methods of generating FM signals. Explain Armstrong method of generating FM signals with a neat block schematic diagram.

b) Draw the spectral representation of FM wave and derive the expression the Transmission bandwidth. [5+5]

8.a) Draw the AM receiver model and determine the signal to noise ratio of AM system.

b) What is the noise equivalent band width? Discuss the trade of between bandwidth and S/N ratio. [5+5]

OR

9. Explain the following:
   a) Resistive noise source.
   b) Shot noise.
   c) In phase and quadrature phase components and its properties.
   d) Noise Figure. [10]

10.a) Explain the operation of Superhetrodyne receiver with a neat schematic diagram.

b) Explain the terms:
   i) Automatic Gain Control (AGC).
   ii) Amplitude limiting
   iii) Squelch circuit. [5+5]

OR

11.a) Compare the pulse modulation systems and continuous modulation systems.

b) What is Multiplexing? What are the advantages of Multiplexing? Explain how do you generate Time Division Multiplexing (TDM) signals. [5+5]

---ooOoo---

Code No: 115AK

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, November - 2015
ANALOG COMMUNICATIONS
(Electronics and Communication Engineering)

COLLEGE OF ENGG. & TECH. LIBRARY SECUNDERABAD

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A **(25 Marks)**

1.a) What is Amplitude modulation? Define modulation index of an AM signal. [2]
b) Draw the Amplitude Modulation waveforms with modulation index (m)=1, m<1, m>1. [3]
c) Compare AM with DSB-SC and SSB-SC. [2]
d) For 100% modulation what is the relationship between the voltage amplitudes of the side band. [3]
e) Define the term modulation index for AM and FM. [2]
f) Derive the formula for instantaneous value of FM voltage. [3]
g) What is the need of pre-emphasis and de-emphasis in FM transmission? [2]
h) Calculate the thermal noise power appearing across a 20kΩ resistor at 25^0C temperature with an effect noise bandwidth of 10KHZ. [3]
i) Explain single polarity and double polarity PAM. [2]
j) Explain simple and delayed AGC. [3]

PART - B **(50 Marks)**

2. What is the principle of amplitude modulation? Derive expression for the AM wave and draw its spectrum. [10]

OR

3. For an Am DSBFC wave with peak unmodulated carrier voltage V_c=10Vp, a load resistance R_L= 10 Ω and a modulation co efficient m = 1. Determine
a) Power of carrier, upper and lower side band
b) Total power of modulate wave
c) Total sideband power
d) Draw the power spectrum. [2+2+3+3]

4. With a neat diagram explain how a SSB wave is generated using Phase Discriminator method with only USB and rejecting the LSB. [10]

OR

5. Derive an expression for SSB Modulated wave for which upper sideband is retained. [10]

6. Explain the principle of Angle Modulation. Derive and explain phase deviation, Modulation index, frequency deviation and percent modulation. [10]

OR

7. Derive the expression for the frequency modulated signal. Explain what is meant by narrowband FM and wideband FM using the expression. [10]

8. Draw and explain the pre-emphasis and de-emphasis circuits with a neat diagram. What is their function? [10]

OR

9. Derive the effective noise temperature of a cascade amplifier. Explain how the various noises are generated in the method of representing them. [10]

10.a) Draw and explain block diagram of double conversion FM receiver.

b) What do you mean by pulse modulation and define types of pulse modulation? [6+4]

OR

11. What is AGC? Draw and explain a simple AGC circuit and what are the different types of AGC explain them. [10]

---ooOoo---

N3

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

B.Tech III Year I Semester Examinations, 2015

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Model Question Paper-1

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is Compulsory which carries 25 marks .Answer all questions in Part A. Part B consists of 5 Units.

Answer any one full question from each unit. Each question carries 10 marks and may have a,b,c, as sub Questions

PART-A

1. Answer all the following questions:

a) Define Modulation. List out different types of modulations.

b) State how a DSB-SC signal may be generated.

c) In the filter method of generation of SSB-SC signal, why is it necessary that the message signal should have a hole near the origin in its spectrum?

d) Write down an expression for the time-domain representation of a VSB signal.

e) Define the term modulation index for FM in the case of single-tone modulation.

f) Compare AM with FM. Which is more immune to noise and why?

g) What is white noise? Sketch the PSD and ACF of white noise.

h) Define noise figure and noise temperature.

i) What do you mean by synchronization in PAM systems?

j) What is meant by tracking error?

PART-B

Answer all the following questions **10x5=50**

2. Show, giving a mathematical proof, how a square-law device can be used to generate an AM signal. Give complete diagram of the signal input and output arrangements. Draw the output spectrum.

OR

3. Explain Frequency Division Multiplexing with a neat diagram.

4. i) Find the percentage of power saved in SSB when compared with AM system.

ii) Why VSB system is widely used for TV broadcasting - Explain?

iii) Why SSB transmission is preferred to DSB-SC?

OR

5. Explain the method of Demodulation of an AM-SSB-SC signal.
6. Explain how a PLL can be used as an FM demodulator.

OR

7. Derive the expression for the FM signal under Tone Modulation and derive the expression its bandwidth.
8. Derive the canonical representation of the narrow band noise. Prove that both the in phase noise $n_c(t)$ and quadrature noise $n_s(t)$ have the same power spectral density.

OR

9. Derive the Noise figure & Equivalent noise temperature of a cascaded network.
10. Derive expressions of Signal to Noise Ratio for an DSB system using coherent demodulation.

OR

11. (a) Draw the block diagram of a Super Heterodyne receiver, and explain the operation of each stage of the receiver.

    (b) A super Hetero dyne receiver is tuned to receive a 1000KHz carrier amplitude modulated by 1KHz sine wave. Assuming the IF of the receiver to be 455KHz, and the frequency components at the input and output of the IF amplifier. Assume the IF bandwidth to be 10 KHz.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

B.Tech III Year I Semester Examinations, 2015

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Model Question Paper-2

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is Compulsory which carries 25 marks .Answer all questions in Part A. Part B consists of 5 Units.

Answer any one full question from each unit. Each question carries 10 marks and may have a,b,c, as sub Questions

PART-A

1. Answer all the following questions:

a) What is modulation index? What happens if it is greater than unity?

b) What is diagonal clipping? How can it be avoided?

c) Discuss the advantages and disadvantages of SSB-SC transmission.

d) Sketch the spectrum of the VSB signal that is given as input to the video detector of a TV receiver.

e) Define frequency modulation and phase modulation.

f) Write a short note on transmission bandwidth of FM wave.

g) What is the origin of thermal noise?

h) Define $(SNR)_O$, $(SNR)_C$, and figure of merit.

i) List the drawbacks of PAM.

j) Distinguish between simple AGC & delayed AGC.

PART-B

Answer all the following questions **10x5=50**

2. Explain the generation of Am wave using Switching Modulator.

OR

3. What are the different types of DSB-SC modulators? Explain them.

4. Explain the detection of VSB signal using envelope detector.

OR

5. Derive the time domain expression for an SSB wave.

6. (a) Explain how PM signal can be generated from FM signal. Justify with the necessary mathematics and give the block diagram representation of the corresponding implementation.

(b) For the FM signal $X(t) = 20.\text{Cos}[2\pi x10^6 t+2.\text{Sin}(2\pi x10^4 t)]$, plot the magnitude spectrum, as per Carson's rule. It is given that $J_0(2) = 0.224$; $J_1(2) = 0.577$; $J_2(2) = 0.353$; $J_3(2) = 0.129$.

OR

7. Explain how a Varactor Diode is used to generate FM signal. Explain with the necessary mathematical equations.
8. Prove that the cross-spectral densities of the quadrature components of narrow band noise are purely imaginary, as shown by

$$S_{NcNs}(f) = -S_{NcNs}(f) = \begin{cases} j[S_N(f+fc)-S_N(f-fc)]; & -B \le f \le B \\ 0 & \text{;elsewhere} \end{cases}$$

OR

9. Derive the expression for Noise bandwidth.
10. a) Explain the generation of PAM.
    b) Explain the characteristics of Super heterodyne receivers

OR

11. Explain FM receiver of the superheterodyne type.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

B.Tech III Year I Semester Examinations, 2015

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Model Question Paper-3

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is Compulsory which carries 25 marks .Answer all questions in Part A. Part B consists of 5 Units.

Answer any one full question from each unit. Each question carries 10 marks and may have a,b,c, as sub Questions

PART-A

1. Answer all the following questions:

a) A carrier signal is sinusoidal modulated to a depth of μ=0.8. What is the percentage of the total power of the modulated signal is in the two sidebands?

b) Sketch the spectrum of an AM signal assuming sinusoidal modulation with a modulation index of less than unity.

c) Draw the spectrum of an LSSB-SC signal. Write down an expression for this spectrum in terms of that of the message signals.

d) Explain briefly the basic principle of FDM.

e) Write about the relationship between FM and PM.

f) How is a PLL useful in detecting FM signals?

g) Draw the block diagram of the model used for the channel and the receiver to study the noise performance of AM system.

h) Define shot noise.

i) What is multiplexing? Differentiate TDM & FDM.

j) A TRF receiver is turned to 1000 KHz AM radio broadcast signal by a variable tuned circuit with 1 KHz bandwidth. Find the bandwidth when receiver is returned to 1550 KHz and 550 KHz. Determined the recovered baseband.

PART-B

Answer all the following questions **10x5=50**

2. (a) Explain about the quadrature null effect of coherent detector.

(b) In DSB-SC, suppression of carrier so as to save transmitter power results in receiver complexity - Justify this statement.

OR

3. Explain the operation of an Envelope Detector. Explain about Diagonal Clipping in a diode detector. How to avoid it?
4. (a) State and prove the properties of Hilbert Transform of a Signal x(t).
   (b) Find the Hilbert Transform of
   i. $x(t)=\frac{\sin t}{t} \cdot \cos 200\pi t$
   ii. $x(t)=\frac{\sin t}{t} \cdot \sin 200\pi t$

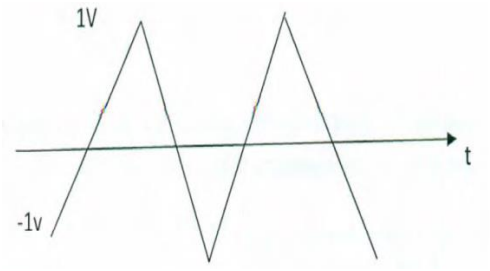
OR

5. Derive the time domain expression of VSB wave.
6. For an FM Reactance Modulator, derive the expression for the:
   a) Inductive reactance offered
   b) Capacitive reactance offered.

OR

7. a) A base band signal m(t) as shown below figure 1 modulates a sinusoidal carrier of frequency 100MHz, in its
   i. phase
   ii. Frequency.

The separation between the adjacent peaks of m(t) is 20mSec.The respective Phase sensitivity and Frequency sensitivity factors are 10π and $2\pi x10^5$. Find the Maximum and Minimum frequency in the corresponding FM and PM signals.



b) Justify that one form of Angle Modulation can be obtained from the other, with the necessary explanation.

8. Derive the Signal to noise ratios for coherent reception with SSB modulation.

OR

9. What is noise triangle with respect to angle modulation?

10. (a) What is an Amplitude Limiter? Explain its operation with a neat circuit diagram.

    (b) What is automatic gain control? What are its functions?

OR

11. (a) With the aid of the block diagram explain TRF receiver. List out the advantages and disadvantages of TRF receiver.

    (b) Define and distinguish between PTM and PAM schemes. Sketch and explain their waveform for a single tone sinusoidal input signal.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

B.Tech III Year I Semester Examinations, 2015

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Model Question Paper-4

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is Compulsory which carries 25 marks .Answer all questions in Part A. Part B consists of 5 Units.

Answer any one full question from each unit. Each question carries 10 marks and may have a,b,c, as sub Questions

PART-A

1. Answer all the following questions:

a) State the advantages and disadvantages of AM. Where it is used?

b) Explain briefly the quadrature null effect in DSB-SC Demodulation.

c) A DSB-SC modulated signal and carrier signal are given as $s(t)=(\cos 2\Pi*500t+2\cos 2\Pi*1000t)$, $c(t)=50\cos 2\Pi*10^5t$ respectively. Find the expressions for USB and LSB components of the modulated signal and sketch their spectra.

d) State the applications of VSB transmission.

e) Draw the block diagram for indirect method of generating an WBFM signal.

f) An FM system has a frequency deviation of 30KHz. The modulating frequency is 3 KHz. Calculate the bandwidth and modulation index.

g) Define narrowband noise and give the expression for narrowband noise in terms of inphase and quadrature component.

h) Define and explain the term noise equivalent bandwidth of a filter.

i) Two signals $x(t) = \cos 2\pi t$ and $y(t) = \cos \pi t + 2\cos 2\pi t$ are to be sampled and to be transmitted using TDM. Find the minimum bandwidth required to transmit the multiplexed signal.

j) List the factors on which selectivity depends.

PART-B

Answer all the following questions **10x5=50**

2. Justify that a Costa's loop can be used for carrier Acquisition and for demodulation of AM-DSB-SC signal also.

OR

3. A Tone modulated AM signal with a modulation index of “m" and base band signal frequency of ω_m is detected using Envelope Detector, whose time constant is RC. For effective demodulation, show that $\frac{1}{RC} \geq \frac{m\omega_m}{\sqrt{1-m^2}}$.
4. Explain the generation of vestigial side band modulated signal.

OR

5. Discuss the phase shift method of generating AM-SSB-SC signal, consisting of the lower side band, with a neat block diagram.
6. Derive the expression for narrow band FM. Explain its generation using a neat block diagram and give its phasor representation.

OR

7. Explain the detection of FM using Zero crossing detector.
8. (a) A DSB-SC signal with additive white noise is demodulated by a synchronous detector using a local carrier of $2\text{Cos}(\omega_c t + \Phi)$. Show that the figure of merit of the receiver is $\text{Cos}^2 \Phi$.

   (b) Derive the expression for the transfer function of a Pre-emphasis and De- emphasis circuit.

OR

9. (a). Discuss the method of generation of a PWM signal.

   (b) How a PPM signal can be generated from a PWM signal.
10. (a) Explain about the Image frequency and Image frequency rejection of a radio receiver.

    (b) Explain about Double Spotting.

OR

11. Explain Time division multiplexing with a neat block diagram.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

B.Tech III Year I Semester Examinations, 2015

ANALOG COMMUNICATIONS

(Electronics and Communication Engineering)

Model Question Paper-5

Time: 3 hours Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is Compulsory which carries 25 marks .Answer all questions in Part A. Part B consists of 5 Units.

Answer any one full question from each unit. Each question carries 10 marks and may have a,b,c, as sub Questions

PART-A

1. Answer all the following questions:

a) Write the expression for AM modulation and draw the spectrum.

b) Compare DBS-SC modulation with SSB-SC modulation.

c) Write short notes on need for modulation.

d) Define multiplexing and its types.

e) Compare NBFM and WBFM.

f) Define Angle modulation and state its advantage over Amplitude modulation.

g) Name the important components of external noise and internal noise.

h) Explain the need for pre-emphasis and de-emphasis in case of FM systems.

i) Compare various pulse analog modulation methods.

j) What exactly, does a noise limiter do in AM receiver and how?

PART-B

Answer all the following questions **10x5=50**

2. What is the necessity of synchronous Carrier in the coherent detection of a Suppressed carrier signal? Explain in detail, with the necessary mathematical treatment.

OR

3. Explain how an AM signal can be generated using Non-Linear Modulation, and derive the necessary equations.
4. Explain the generation of SSB modulated wave using Frequency discrimination method.

OR

5. Explain the frequency description of VSB wave.

6. Derive the expression for Wide band FM.

OR

7. Explain the operation of the balanced slope detector using a circuit diagram and draw its response characteristics. Discuss in particular the method of combining the outputs of the individual diodes. In what way is this circuit an improvement on the slope detector and in turn what are the advantages?
8. (a) Derive the expression for the Figure of Merit for an envelope detector used to detect an AM-DSB-Full Carrier signal, under low noise case.

   (b) An AM receiver operates with a tone modulation and the modulation index is 0.3. The message signal is $20.\text{Cos}1000\pi t$.

   i. Compute the figure of Merit.

   ii. Determine the improvement in O/P signal to Noise Ratio if the modulation index is increased to 70%.

OR

9. Derive the expression for the Figure of merit for an FM receiver.
10. (a) What is the fundamental difference between pulse modulation, on the one hand, and frequency and amplitude modulation on the other?

    (b) What is pulse width modulation? What other names does it have? How is it demodulated?

OR

11. Describe the generation and demodulation of PPM with the help of block diagram and hence discuss its spectral characteristics.

Code No: R15A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

Digital Design Through Verilog

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A (25 Marks)

1. (a) Differentiate between different data types in Verilog.(2M)
(b) Explain briefly about the operators in Verilog. (3M)
(c) Discuss about strength contention in gate primitives? (2M)
(d) Explain 'case' statement with syntax in verilog. . (3M)
(e) What is intra-assignment delay? (2M)
(f) Explain assign-deassign construct in Verilog. (3M)
(g) How do you model path delays in Verilog? (2M)
(h) What are the differences between basic and resistive transistor switch primitives. (3M)
(i) What is a feedback model? (2M)
(j) What is test bench. (3M)

PART – B (50 Marks)

SECTION – I

2. a) Explain the keyword module with an example.(5M)
b) Describe in detail about the system tasks. (5M)

(OR)

3. a) Differentiate between synthesis and simulation. (5M)
b) Explain levels of abstraction in digital design with examples. (5M)

SECTION – II

4. a) Prepare the Verilog module of 4-bit binary adder using full adder module. (5M)
b) Explain continuous assignment structures with examples. (5M)

(OR)

5. a) Write short notes on Tri state gates and delays associated with them. (5M)
b) Write Verilog code and test bench of 4 to 1 multiplexer using ternary operator. (5M)

SECTION – III

6. a) Design a Verilog module of 4 bit left/right shift register using for loop. (5M)
b) Write short notes on the following: (5M)
i) parallel blocks ii) Force-release iii) forever loop

(OR)

7. a) Write Verilog description of JK flip flop with preset and clear facility. (5M)
b) Differentiate between blocking and
non blocking assignments with examples. (5M)

SECTION – IV

8. a) Design a 3 input CMOS NAND gate. Write the Verilog code and test bench for it. (5M)
b) Explain about compiler directives and path delays in Verilog. (5M)

(OR)

9. a) What is the importance of user defined primitives? Explain. (5M)
b) Implement a RAM cell using CMOS switch and describe it using Verilog. (5M)

SECTION – V

10. a) Explain the basic functional registers. (5M)
b) Explain combinational circuit testing with an example. (5M)

(OR)

11. a) Show the Verilog code of the following up-down counter. The counter has a u input that controls its count direction. If u is 1, it counts 010, 011, 101, 011, 111, 001 ... . If u is 0, it counts this same sequence in the opposite direction. (5M)
b) Explain sequential circuit testing with an example. (5M)

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Code No: R15A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations, November 2017

Digital Design Through Verilog

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A **(25 Marks)**

1. (a) Describe the system tasks in Verilog. 2M
(b) Explain briefly about the module in Verilog. 3M
(c) Discuss about strength contention in gate primitives? 2M
(d) Explain briefly about wand, wor and tri type nets. 3M
(e) What is the importance of disable construct in Verilog. 2M
(f) Differentiate between case, casex and casez statements. 3M
(g) What is the syntax of CMOS transmission gate. 2M
(h) What are the differences between basic and resistive transistor switch primitives. 3M
(i) What is a capacitive model? 2M
(j) Differentiate between different assertion statements. 3M

PART – B **(50 Marks)**

SECTION – I

2. a) Explain the following terms: 5M
i) Simulation ii) Synthesis
b) Discuss in detail about the Lexical tokens. 5M

(OR)

3. a) Explain levels of abstraction in digital design with examples. 5M
b) Explain in detail about functional verification. 5M

SECTION – II

4. a) Design 3 to 8 decoder using 2 to 4 decoders and Write Verilog Code for the same. 5M
b) Write short notes on continuous assignment statements with delays. 5M

(OR)

5. a) Write a Verilog code for D latch using NAND gates. 5M
b) Explain in detail about the operators in Verilog. 5M

SECTION – III

6. a) Differentiate between blocking and non blocking assignments with examples. 5M

b) Explain procedural assignment blocks with suitable verilog modules 5M

(OR)

7. Design a full adder module with time delay assignment through parameter declaration. Also write the test bench module and verify the simulation results. 10M

SECTION – IV

8. a) Design a 3 input CMOS NOR gate. Write the Verilog code and test bench for it. 6M

b) Explain about compiler directives and module parameters in Verilog. 4M

(OR)

9. a) What is the importance of user defined primitives? Explain. 5M

b) Implement 4 to 1 multiplexer using CMOS transmission gates and describe it using Verilog. 5M

SECTION – V

10. a) Explain the sequential models with neat sketches 5M

b) Explain combinational circuit testing with an example. 5M

(OR)

11. a) Write a 32bit word register file in Verilog which reads its data from a file named data.mem. It has a 5-bit address input named index and a read input signal. When the read input is 1, the output of the memory is equal to the data written in the index address of the register file, otherwise the output equals 8'bZZ. 5M

b) Explain sequential circuit testing with an example. 5M

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12

R13

Code No: 114AF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, May - 2017

DIGITAL DESIGN USING VERILOG HDL

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Write a short note on keywords.	[2]
b)	Write about white space character with an example.	[3]
c)	Illustrate an example to design tri type net.	[2]
d)	Explain the gate Delay.	[3]
e)	What are local variables?	[2]
f)	Write about 'Repeat' Construct.	[3]
g)	Define Computer Directives.	[2]
h)	Define time delay with example.	[3]
i)	Write about switch primitives.	[2]
j)	Draw the basic RAM Cell Diagram.	[3]

PART-B

(50 Marks)

2.a)	Explain in detail the Levels of Design Description.	
b)	Explain the concept of numbers in Language constructs.	[5+5]
	OR	
3.a)	Explain the Strings with suitable examples.	
b)	Explain the Simulation and Synthesis in Verilog HDL.	[5+5]
4.a)	Describe the model structures with an example.	
b)	Design a 3 to 8 decoder.	[5+5]
	OR	
5.a)	Discuss the tri state gates with an example.	
b)	Write about array of instances of primitives.	[5+5]
6.a)	Explain with an example how 'while' construct is used.	
b)	Write briefly about functional bifurcation.	[5+5]
	OR	
7.a)	Design an 8-bit adder module using for loop.	
b)	Explain disable construct with an example.	[5+5]

8.a) Discuss Basic Transistor Switches.
b) Explain File Based Tasks and Functions. [5+5]

OR

9.a) Explain the Strength Contention with Trireg Nets.
b) Explain the Hierarchical Access. [5+5]

10.a) Explain the Sequential Model-Feedback Model.
b) Write about Assertion Verification. [5+5]

OR

11.a) Explain the Static Machine Coding.
b) Explain the Sequential Circuit Testing. [5+5]

---ooOoo---

Code No: 114AF **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, October/November - 2016
DIGITAL DESIGN USING VERILOG HDL
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART - A **(25 Marks)**

1.a)	Define Keywords and Identifiers.	[2]
b)	Define parameters and memory operators.	[3]
c)	Define strengths and content resolution.	[2]
d)	What is continuous assignment structure?	[3]
e)	Explain assignments with delays.	[2]
f)	Draw a simulation flow chart.	[3]
g)	Explain the operation of PMOS switch.	[2]
h)	Explain basic transistor switches.	[3]
i)	Explain capacitive model.	[2]
j)	What is sequential circuit testing?	[3]

PART – B **(50 Marks)**

2. Explain with examples about:
a) Display tasks b) Strobe tasks c) Monitor tasks. [3+3+4]

OR

3.a) Using example, explain about concurrent and procedural statement with syntaxes.
b) Explain the components of a Verilog module with block diagram. [5+5]

4.a) Write a Verilog code for tri-state devices.
b) Explain clocked RS filp-flop Verilog module and test bench. [5+5]

OR

5.a) Design a Verilog module of a 4-bit bus switcher at the data flow level.
b) Explain about operator priority with examples. [5+5]

6.a) Explain blocking and non-blocking statement with examples.
b) Write Verilog code using case statement for any one example. [5+5]

OR

7.a) Explain event construct in a module.
b) Explain stratified event queue. [5+5]

8.a) Design Verilog module for CMOS filp-flop.
b) Explain about module paths. [5+5]

OR

9.a) Explain overriding parameters.
b) Design Verilog module using path delay. [5+5]

10.a) What are the various sequential memory storage models? Explain in detail.
b) How the memory initialization carried out in Verilog? Explain with the help of an example. [5+5]

OR

11.a) With the help of an example explain about the resetting sequence of controller.
b) Write a test bench for moore detector to control the delay. [5+5]

---ooOoo---

Code No: 114AF

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May-2015
DIGITAL DESIGN USING VERILOG HDL
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Write difference between tasks and functions.	[2M]
b)	Illustrate with an example Array of Instances of Primitives.	[3M]
c)	What are Tristate gates?	[2M]
d)	Mention data types used in Verilog HDL.	[3M]
e)	Write any two sequential models can be used.	[2M]
f)	Write about bidirectional gates.	[3M]
g)	What are parallel blocks?	[2M]
h)	What are time delays with switch primitives?	[3M]
i)	Draw the diagram of NAND gate using CMOS switches.	[2M]
j)	Write Verilog code using Case statement.	[3M]

PART-B

(50 Marks)

2. Explain the following "lexical conventions" with examples.
a) White space b) strengths c) Operators [3+3+4]

OR

3.a) Write a short notes on concurrency and functional verification.
b) Explain port Declaration with an example using Verilog code. [5+5]

4.a) Classify and explain strengths and contention resolution.
b) Write Verilog code for 1 to 4 demultiplexer module by using 2 to 4 decoder? [5+5]

OR

5.a) Write Verilog module for a positive edge triggered flip flop with test bench.
b) Explain how the ALWAYS statements are used in Verilog. [5+5]

6.a) Design Verilog module Event construct for a serial data receive and test bench for the same.
b) Design a counter module and test bench to illustrate the use of WAIT. [5+5]

OR

7.a) Describe procedural continuous assignment statements assign, de assign, force and release.

b) Explain the compiles directives in detail. [5+5]

8.a) Design CMOS switch of parallel combination.

b) Explain and specify blocks of Path Delay Modeling. [5+5]

OR

9.a) Write the code for CMOS switch of parallel combination.

b) Briefly explain combinational and sequential UDPs in Verilog. [5+5]

10.a) Write the verilog code for basic functional unit of a dynamic shift register.

b) Write a short note on Design verification. [5+5]

OR

11.a) Briefly explain any one method used for sequential circuit testing.

b) Write Verilog module for 8-bit comparator with test bench. [5+5]

---ooOoo---

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MALLAREDDY COLLEGE OF ENGINNERING AND TECHNOLOGY

DEPARTMEMNT OF ELECTRONICS AND COMMUNICATION ENGINNERING

B. Tech II year – II Semester Examinations, Model Paper-1

DIGITAL DESIGN USING VERILOG HDL

Time: 3 Hours **Max. Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consist of 5 units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions

Part –A **(25 Marks)**

1. a) Define gate level modelling. [2M]
b) What are tristate gates? [3M]
c) Define: - [2M]
(i) Unary operators (ii) Ternary operators
d) Give the syntax of repeat construct. [3M]
e) Write the Verilog module for repeat construct. [2M]
f) Define keyword in Verilog HDL. [3M]
g) Define net delay. [2M]
h) Write the syntax of even construct. [3M]
i) Define path delay. [2M]
j) What is functional register? [3M]

Part- B **(50Marks)**

2. Explain different levels of design description in Verilog.

OR

3. Define the terms relevant to Verilog HDL
(i) Simulation
(ii) PLI
(iii) System tasks

4. Write short notes on the following with examples.
(i) Logical operators
(ii) Conditional operator
(iii) Arithmetic operators

OR

5. Write the Verilog code for 4 X1 Multiplexer using the tristate buffer in the gate level modelling.

6. Design Verilog module for an edge triggered D Flip flop in the data flow model.

OR

7. Explain blocking and Non-blocking statements with examples.

8. Write short notes on time delays with switch primitives relevant to switch level modelling.

OR

9. Design half adder using CMOS switches.

10. Draw the block diagram of master slave flip flop constructed using latches and Verilog code is to be written.

OR

11. Write the Verilog code for 4 bit ALU also obtain its test bench and simulation results.

MALLAREDDY COLLEGE OF ENGINNERING AND TECHNOLOGY

DEPARTMEMNT OF ELECTRONICS AND COMMUNICATION ENGINNERING

B. Tech II year – II Semester Examinations, Model Paper -2

DIGITAL DESIGN USING VERILOG HDL

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consist of 5 units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions

Part –A **(25 Marks)**

1. a) Explain the different levels of design description in Verilog. [2M]
b) What are the different levels of PLI? [3M]
c) What are delays? [2M]
d) Define i) Unary operators ii) Binary operators. [3M]
e) Give the syntax of always construct. [2M]
f) Give the syntax of case statement. [3M]
g) Explain type declaration for parameters. [2M]
h) Explain automatic function. [3M]
I) Write the function for fork join construct [2M]
j) Define setup time [3M]

Part- B **(50Marks)**

2. a) Define and explain the following terms pertaining to Verilog HDL.
(i) Scalars and vectors
(ii) PLI

b) Define and explain the following terms relevant to Verilog HDL language elements.
(i) White space characters
(ii) Comments
(iii) Exercises

OR

3. a) What is Verilog HDL? Describe in brief, the basic modelling styles supported by Verilog HDL.
b) What are the data types available in Verilog HDL? Discuss them with necessary syntax and an example.

4. a) Describe the following relevant to gate level modelling with necessary syntax and example.
(i) Gate delays (ii) Array of instances

b) Give a gate level description of a 2-4 decoder circuit with relevant logic diagram and Verilog HDL source code.

OR

5. a) Describe the following relevant to gate level modelling with necessary syntax and example.
(i) Module structure (ii) Strengths and contention resolution

b) Present the gate level description of a master salve Flip flop circuit with relevant logic diagram and Verilog HDL source code.

6. a) Describe the following relevant to behavioural modelling with necessary syntax and example
(i) Timing controls (ii) Case statement

b) Give the behavioural description of a JK Flip flop circuit using an always statement with necessary logic diagram and Verilog HDL source code.

OR

7. a) Discuss the following related to behavioural level modelling with necessary syntax and example.
(i) Block statement (ii) Case statement

b) What is the difference between a sequential block and a parallel block? Explain using an example. Can a sequential block appear with in a parallel block?

8. a) Describe the continuous assignment feature of Verilog HDL with suitable example.
b) What are the switch level primitives and give their instantiations. Draw the basic switch circuit and its Verilog HDL code.

OR

9. a) Define user defined primitives with their syntax. Give an example of 4 to 1 multiplexer built using UDPs.
b) Explain about CMOS switch and Bi-directional gates related to switch level modelling in Verilog HDL.

10. a) Explain the concept of state machine chart realization through MUX and PLD devices.
b) Draw an ASM chart to describe a state machine that detects a sequence of three logic is occurring at the input and that asserts a logic 1 at the output during the last state of the sequence. Write a two process Verilog HDL description to the state machine.

OR

11. a) Draw the state diagram and state machine chart for a two bit UP/DOWN counter having a control input ‘C’ in such a way that if C=1 up-counting and C=0 down-counting. The counter should generate an output Z=1 whenever count becomes minimum or maximum.
b) Write notes on modelling a Moore FSM.

MALLAREDDY COLLEGE OF ENGINNERING AND TECHNOLOGY

DEPARTMEMNT OF ELECTRONICS AND COMMUNICATION ENGINNERING

B. Tech II year – II Semester Examinations, Model Paper -3

DIGITAL DESIGN USING VERILOG HDL

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consist of 5 units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions

Part –A **(25 Marks)**

1). a) Write short notes on verilog HDL.

b) Write about applications of ASIC design

c) Explain about tristate gates.

d) Write a verilog code using data flow model.

e) Draw a flowchart for execution of IF ELSE loop.

f) Draw a 2 to 4 decoder using enability and write the design module in behavioral model.

g) Explain about CMOS inverter.

h) Write about Hierachical access.

i) Draw a block diagram of moore model.

j) Explain about serial data transmission in UART design.

PART-B **(50 Marks)**

2).a) Explain the components of a verilog module with a block diagram.

b) Differentiate between simulation and synthesis.

(OR)

3). a) Explain about LEXICAN TOKENS in verilog.

b) Explain about concurrency.

4).a) Design a JK FLIP FLOP using NAND gates.

b) Write a verilog code for JK FLIP FLOP using NAND gates.

(OR)

5).a) Explain a module with example using verilog code.

b) Explain port declaration with an example using verilog code.

6). a) Explain continuous assignment structure with examples.

b) Explain combining assignment and net declaration with examples.

(OR)

7).a) Write the verilog code for AOI in behavioral model.

b) Write the verilog code for 4 bit down counter using ternary operator in behavioral model.

8). a) Explain edge sensitive path using an example.

b) Explain about over riding parameters.

(OR)

9).a) Explain type declaration for parameters

b) Explain specify mode for path delays.

10).a) Explain dice game with block diagram.

b) Explain dice game using flow chart

(OR)

11). a) Explain combinational logic operation of XC300FPGA.

b) Explain XC3000 series FPGA flip flop with clock enable.

MALLAREDDY COLLEGE OF ENGINNERING AND TECHNOLOGY

DEPARTMEMNT OF ELECTRONICS AND COMMUNICATION ENGINNERING

B. Tech II year – II Semester Examinations, Model Paper-4

DIGITAL DESIGN USING VERILOG HDL

Time: 3 Hours **Max. Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consist of 5 units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions

Part –A **(25 Marks)**

1) a) Define synthesis and simulation. [2M]
   b) What are tristate gates? [3M]
   c) write a short notes: - [2M]
   (i) Ternary operators
   d) write a short notes on always construct. [3M]
   e) Write the Verilog module for repeat construct. [2M]
   f) Define keyword in Verilog HDL. [3M]
   g) Define net delay. [2M]
   h) Write the syntax of even construct. [3M]
   i) Define setup and hold time. [2M]
   j)define moore and melay machine? [3M]

Part- B **(50Marks)**

2) i)Explain different levels of design description in verilog.
   ii)Explain port declaration with an example.

or

3) Design a 1x4 demultiplexer module by using 2x4 decoder and write NAND gates.
4) i)Designa JK flip flop using NAND gate and write verilog code for it.
   ii)Design T-flipflop using NAND gates.

or

5) i) write a verilog module using case statement and implement 1x16 multiplexer.
6) Design module to convert angle in radians to one degrees with explanation.

or

7) Write the verilog code for half substractor using CMOS switches.
8) I) Explain $random function with example?
   ii)Explain type declaration for parameter ?

or

9) write a short notes on moore 101 sequence detector and write the verilog code for the same.

10) write a verilog module for 4-bit ALU also obtain its test bench and simulation results.

or

11) write in detail about assertion verification and also give its benefits.

MALLAREDDY COLLEGE OF ENGINNERING AND TECHNOLOGY

DEPARTMEMNT OF ELECTRONICS AND COMMUNICATION ENGINNERING

B. Tech II year – II Semester Examinations, Model Paper -5

DIGITAL DESIGN USING VERILOG HDL

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consist of 5 units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions

Part –A **(25 Marks)**

1. a) Give the functioning of "$ monitor" on system task? [2m]

   b) What is the difference between Scalars and vectors in module? [3m]

   c) Explain different levels of design descriptions in verilog ? [2m]

   d) Define Strength and list out types of Strengths. [3m]

   e) Write short note on Blocking and Non-Blocking statement. [2m]

   f) Give the syntax of the following (1) If and If-else, (2) Forever loop. [3m]

   g) What are Bi-directional Gates and List them. [2m]

   h) Define automatic function? Explain? [3m]

   i) Explain LFSR and MISR? [2m]

   j) Define (1)Setup hold, (2) Width, (3) Hold time. [3m]

Part- B **(50Marks)**

2) a) What are LEXICAL TOKENS and Explain.

OR

3) b) Explain about the Numbers System in verilog.

4) a) Design T-FlipFlop using NAND Gate

OR

5) b) (1) Explain continuous assignment structures with examples?

(2) Explain Concurrent Statement in data flow model?

6) a) (1) Write the difference between begin-end Block and Fork join Block

(2) Write a short note on functional Bifurcation

OR

7) b) Write a verilog code for up counter using behavioral model.

8) a) (1) Design a half subtractor using CMOS Switches.

(2) Write a verilog code for 4 bit full adder with carry look ahead.

OR

9) b) Define the following terms.

(1) Module parameter,

(2) File based tasks and functions,

(3) Compiler directives.

10) a) What are the various Sequential memory storage models? Explain in detail?

OR

11) b) (1) Write the rules to be followed to declare and to use the bi-directional lines?

(2) Write a verilog module for PLA?

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-I

DIGITAL SYSTEM DESIGN

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1. a. What is the difference between Moore and Mealy machine? (2 M)
   b. What are the limitations and capabilities of FSM? (3 M)
   c. What is fundamental mode model? (2 M)
   d. What are Hazards? (2 M)
   e. What are differences between PLA and PAL? (3M)
   f. Describe the advantages of PLA minimization and folding. (3M)
   g. Explain bridge fault model. (2 M)
   h. Explain the Stuck at faults with an example. (3 M)
   i. What are the principal components of State machine chart? (3 M)
   j. What is a State Machine? (2 M)

PART-B (5*10=50 Marks)

2.a) Find the equivalence partition for the machine shown below

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,0	F,1
E	D,1	E,1
F	C,1	E,1
G	C,1	D,1
H	C,0	A,1

b) Show a standard form of the corresponding reduced machine

OR

3. Explain the following related to sequential circuits with suitable
   a) State diagram b) State Table c) State Assignment

4. A fundamental –mode sequential machine has two inputs, x_1 and x_2 , and two outputs, z_1 and z_2 . z_1 becomes 1 when x_1 changes its value preceded by a change in value in x_2 . z_2 becomes 1 when x_2 changes its value preceded by a change in value in x_1.Once 1, both z_1 and z_2 return to 0 only when both x_1 and x_2 become 0.

MRCET

(i) Derive a minimum-row state table having fast and flicker-free output

(ii) Show a valid assignment (race-free) and write a set of (static) hazard-free exitation and output equations.

OR

5. a).Explain briefly, the occurrence of various types of hazards in digital circuits.

b).Implement a hazard free circuit for the following function:

f (ABCD) =A'BC' +A'B'C + CD'+AC

6. Explain PLA minimization procedure and obtain the minimized expression to be implemented on PLA F = 2021 + 0022 + 1200

OR

7. a) Explain ROM architecture in detail.

b) Design a logic circuit which generates the square of a given three bit binary number. Realize the design using ROM.

8. a) What is the significance of Kohavi algorithm? Explain how it is useful in the detection of faults in digital circuits.

b)Apply Kohavi's algorithm to the given POS function f = $(A+\bar{B})(C+BD)$.

OR

9. a).Explain the Stuck at faults with an example.

b).Draw the circuit which realizes the logic function z= x1 x2 +x3 x4 using AND and OR gates. For the circuits realized above, determine a test vector which denotes SA0 fault on the line 'x2'.

10. Realize the state machine chart for dice controller.

OR

11. With an example, explain the use of ASM charts in the design of digital circuits.

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-II

DIGITAL SYSTEM DESIGN

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1. a) Write short note on incompletely specified Machines. (2M)
   b) Define the terms Terminal state, successor and strongly connected machine. (3M)
   c) What is merger Graph? (2M)
   d) What are races and cycles? (3M)
   e) List the advantages of PLA (2M)
   f) Explain crosspoint faults in PLA. (3M)
   g) With an example explain the principle of operation of path sensitization method. (3M)
   h) What are the different types of faults in combinational circuits? (2M)
   i) What are the salient features of SM chart? (3M)
   j) Define Kohavi algorithm. (2M)

PART-B (5*10=50 Marks)

2. Draw the Minimal State table equivalent to the State table given:

PS	NS,Z	
	X=0	X=1
A	A,1	E,0
B	A,0	E,0
C	B,0	F,0
D	B,0	F,0
E	C,0	F,1
F	C,0	F,1
G	D,0	H,1
H	D,0	H,1

OR

3. Convert the following Mealy machine into a corresponding Moore machine.

PS		
A	B,O	E,O
B	E,O	D,O
C	D,I	A,O
D	C,I	E,O
E	B,O	D,O

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4. Give a state assignment without critical races to each of the following asynchronous machine shown in figure.

q \ x	I_0	I_1	I_2	I_3
A	(A)	C	(A)	B
B	A	(B)	A	(B)
C	(C)	(C)	E	D
D	C	B	(D)	(D)
E	(E)	F	(E)	D
F	E	(F)	A	B

OR

5. a) The output Z of a fundamental-mode , two input sequential circuit is to change from 0 to 1 only when x_2 changes from 0 to 1 while x_1 =1. The output is to change from 1 to 0 only when x_1 changes from 1 to 0 while x_2 =1.

(i) Find a minimum- row reduced flow table, the output should be fast and flicker-free.

(ii) Show a valid assignment and write a set of (static) hazard-free exitation and output equations.

6. Give the PLA realization of the following functions using PLA with 5 inputs, 4 outputs and 8 AND gates.

F1(a,b,c,d) = ∑m(0,1,2,3,11,12,13,14,15,16,17,18,19,27,28,29,30,31)

F2(a,b,c,d) = ∑m(4,5,6,7,8,9,10,11,20,21,22,23,30).

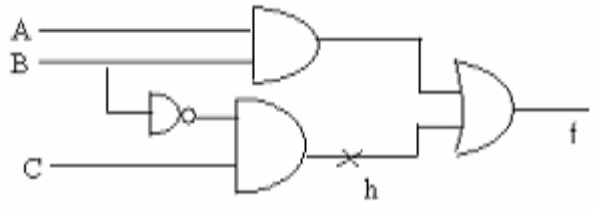
OR

7. Design a 32-bit Adder using Carry Look Ahead Adders.

8. With an example explain the principle of operation of path sensitization method.

OR

9. Using Boolean difference method detect **h** - SA0 fault in the given circuit and derive the test vectors.



10. a) Draw an SM chart to design a binary multiplier.

b) How does the SM chart differ from a software flow chart?

OR

11. Explain in detail the ASM technique of designing a sequential circuit.

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-III

DIGITAL SYSTEM DESIGN

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1 a) Define State equivalence theorem. (2M)
b) What is a flow table? (3M)
c) Write short notes on static hazards. (2M)
d) What are the rules to develop a merger chart? (3M)
e) Explain the programming of ROM. (2M)
f) What is the basic architecture of a PAL? (3M)
g) List out the Boolean difference properties (2M)
h) What is the significance of test pattern generation? (3M)
i) What are the elements of State machine chart? (2M)
j) What is the use of SM charts? (3M)

PART-B (5*10=50 Marks)

2. Construct the compatibility graph and obtain the minimal cover table for the sequential machine described by the state table given.

PS	NS,Z	
	I=0	I=1
1	2,0	3,1
2	1,0	1,1
3	4,1	4,1
4	3,1	6,0
5	1,0	1,1
6	7,0	3,0
7	4,1	4,1

OR

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3. Minimize the following incompletely specified machine using Merger Table method.

PS	NS,Z	
	X = 0	X = 1
A	E,0	B,0
B	F,0	A,0
C	E,-	C,0
D	F,1	D,0
E	C,1	C,0
F	D,-	B,0

4. Design a hazard-free OR-AND network for the boolean function f = ∑m(0,2,6,7).

OR

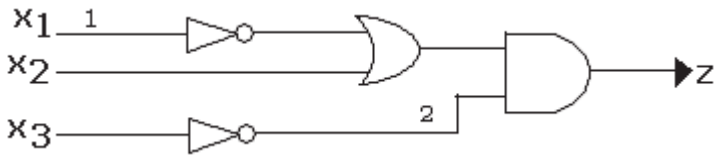
5. a) Explain static,dynamic and essential hazards in digital circuits.

b) Design a hazard free realization for the Boolean expression f(A,B,C,D)=$\sum_m$(2,5,7,8,10,14).

6. Design a BCD adder. **OR**

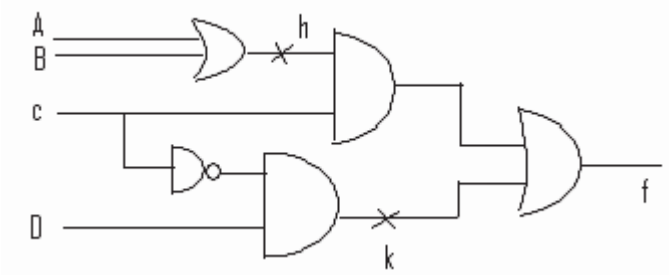
7. Design a 3 bit BCD to Grey code convertor and realize the circuit using PLA and then show how folding reduces the number of cross points on the PLA.

8. Using Path sensitization and Boolean difference method find the test vectors for S-A-0 fault on input line 1 and S-A-1 fault on input line 2 of the circuit given below



OR

9. For the circuit shown below find tests to detect the faults **h** S-A-0 and **h** S-A-1, **k** S-A-0 and **k** S-A-1. Find tests to distinguish between the above faults.



10. Draw an SM chart to design a binary multiplier.

OR

11. Realize the state machine chart for dice controller.

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-IV

DIGITAL SYSTEM DESIGN

Time: 3 hours **Max. Marks: 75**

PART- A (25 Marks)

1. a) Write short note on incompletely specified Machines. (2M)
   b) Differentiate between moore and mealy FSMs. (3M)
   c) What is merger Graph? (2M)
   d) Explain briefly about static and dynamic hazards (3M)
   e) List the advantages of PLA (2M)
   f) Define stuck-at fault. (3M)
   g) With an example explain the principle of operation of path sensitization method. (3M)
   h) What are the different types of faults in combinational circuits? (2M)
   i) What are the salient features of SM chart? (3M)
   j) Define Kohavi algorithm. (2M)

PART – B **(50 Marks)**

SECTION-I

2 a) Reduce the following state table to a minimum number of states. 6M

Present state	Next state X=0	Next state X=1	Output (Z)
A	E	E	1
B	C	E	1
C	I	H	0
D	H	A	1
E	I	F	0
F	E	G	0
G	H	B	1
H	C	D	0
I	F	B	1

b) Discuss about the importance of state reduction in the design of FSMs. 4M

OR

MRCET

3a) Explain the simplification of incompletely specified state table with an example. 6M

b) Discuss about capabilities and limitations of FSMs. 4M

SECTION-II

4. A fundamental –mode sequential machine has two inputs, x_1 and x_2 , and two outputs, z_1 and z_2 . z_1 becomes 1 when x_1 changes its value preceded by a change in value in x_2 . z_2 becomes 1 when x_2 changes its value preceded by a change in value in x_1.Once 1, both z_1 and z_2 return to 0 only when both x_1 and x_2 become 0.

(i) Derive a minimum-row state table having fast and flicker-free output

(ii) Show a valid assignment (race-free) and write a set of (static) hazard-free exitation and output equations.

OR

5. a).Explain briefly, the occurrence of various types of hazards in digital circuits.

b).Implement a hazard free circuit for the following function:

f (ABCD) =A'BC' +A'B'C + CD'+AC

SECTION – III

6 a) Find a minimum row PLA table to implement the following equations. 6M

$x(A,B,C,D) = \sum m(0,1,4,5,6,7,8,9,11,12,14,15)$
$y(A,B,C,D) = \sum m(0,1,4,5,8,10,11,12,14,15)$
$z(A,B,C,D) = \sum m(0,1,3,4,5,7,9,11,15)$

b) Write short notes on the following: 4M

i) PAL ii) ROM

(OR)

7 a) Describe in detail about PLA folding. 5M

b) Implement a 2bit binary adder using ROM. 5M

SECTION – IV

8. With an example explain the principle of operation of path sensitization method.

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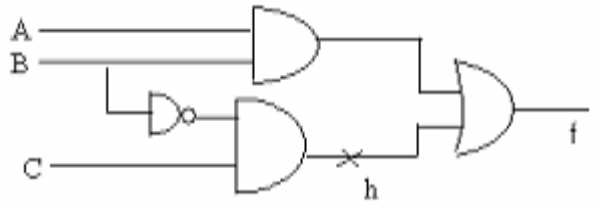
OR

9. Using Boolean difference method detect **h** - SA0 fault in the given circuit and derive the test vectors.



SECTION – V

10. a) Draw an SM chart to design a binary multiplier.

b) How does the SM chart differ from a software flow chart?

OR

11. Explain in detail the ASM technique of designing a sequential circuit.

MRCET

Code No: R15A0411 **R15**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations, November 2017

Digital System Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A (25 Marks)

1. (a) What is a merger chart? 2M
   (b) Differentiate between moore and mealy FSMs. 3M
   (c) Define fundamental mode operation. 2M
   (d) Explain briefly about static and dynamic hazards. 3M
   (e) Explain the difference between ROM and RAM 2M
   (f) Draw the logic diagram of BCD adder. 3M
   (g) Define stuck-at fault. 2M
   (h) Explain the importance of Kohavi algorithm. 3M
   (i) What are the principal components of an SM chart? 2M
   (j) Draw the SM chart of function F=A+BC. 3M

PART – B (50 Marks)

SECTION – I

2. a) Reduce the following state table to a minimum number of states. 6M

Present state	Next state X=0	Next state X=1	Output (Z)
A	E	E	1
B	C	E	1
C	I	H	0
D	H	A	1
E	I	F	0
F	E	G	0
G	H	B	1
H	C	D	0
I	F	B	1

MRCET

b) Discuss about the importance of state reduction in the design of FSMs. 4M

(OR)

3. a) Explain the simplification of incompletely specified state table with an example. 6M
   b) Discuss about capabilities and limitations of FSMs. 4M

SECTION – II

4. a) Obtain a primitive flow table for a circuit with two inputs x1 and x2, and two outputs z1 and z2, that satisfy the following four conditions 6M
   i) when x_1x_2=00, the output z_1z_2=00
   ii) when x_1 =1 and x_2 changes from 0 to 1, the output is z_1z_2=01
   iii) when x_2 =1 and x_1 changes from 0 to 1, the output is z_1z_2=10
   iv) otherwise the output does not change

   b) Describe stable and unstable states in a fundamental mode sequential machine. 4M

(OR)

5. Minimize the following incompletely specified machine using Merger Table method 10M

PS	NS,Z	
	X = 0	X = 1
A	E,0	B,0
B	F,0	A,0
C	E,-	C,0
D	F,1	D,0
E	C,1	C,0
F	D,-	B,0

SECTION – III

6. a) Find a minimum row PLA table to implement the following equations. 6M

   x(A,B,C,D) =∑m(0,1,4,5,6,7,8,9,11,12,14,15)
   y(A,B,C,D) =∑m(0,1,4,5,8,10,11,12,14,15)
   z(A,B,C,D) =∑m(0,1,3,4,5,7,9,11,15)

   b) Write short notes on the following: 4M
   i) PAL ii) ROM

(OR)

7. a) Describe in detail about PLA folding. 5M
   b) Implement a 2bit binary adder using ROM. 5M

SECTION – IV

8. Draw the three bit parity checker circuit. Using the path sensitization method, find the test vectors for SA0 and SA1 faults on each line of the circuit. 10M

(OR)

9. a) Find a minimum set of 'a' and 'b' tests for the two level AND- OR logic circuit represented by the following function by using Kohavi algorithm 6M

$$f_1=(x_1*x_2)+(x_2'*x_4')+(x_1'*x_2'*x_3')$$

b) Explain about bridging fault. 4M

SECTION – V

10. a) Draw the SM chart of Dice game. 6M

b) Write short notes on equivalent SM blocks. 4M

(OR)

11. Draw the SM chart of the binary multiplier controller and Implement it using PLA and Flip-flops. 10M

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MRCET

R15

Code No: R15A0411

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

Digital System Design

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART – A (25 Marks)

1(a) What are the limitations and capabilities of FSM .(2M)
(b) Differentiate between moore and mealy FSMs. (3M)
(c) What is the difference between synchronous and asynchronous circuits? (2M)
(d) What is fundamental mode model . (3M)
(e) Differentiate between PLA and PAL. (2M)
(f) Explain bridge fault model (3M)
(g) Define stuck-at fault. (2M)
(h) Explain the importance of Kohavi algorithm.(3M)
(i) What are the advantages of SM chart over state graphs? (2M)
(j) Define SM chart and its components. (3M)

MRCET

PART – B (50 Marks)

SECTION – I

2. Minimize the following incompletely specified machine using Merger Table method (10M)

PS	NS,Z	
	X=0	X=1
A	E, 0	B, 0
B	F, 0	A,0
C	E, -	C,0
D	F, 1	D,0
E	C, 1	C,0
F	D, -	B,0

(OR)

3a) Reduce the following state table to a minimum number of states.(6M)

Present state	Next state X=0 X=1		Output (Z) X=0 X=1	
A	C	F	0	0
B	D	E	0	0
C	H	G	0	0
D	B	G	0	0
E	E	B	0	1
F	F	A	0	1
G	C	G	0	1
H	C	F	0	0

b) Discuss about the importance of state reduction in the design of FSMs. (4M)

SECTION – II

4a) Determine all the races in the following state table. Indicate which of these are critical and which are not.(6M)

y_1y_2	Y_1Y_2 / x_1x_2 00	01	11	10
00	01	(00)	(00)	01
01	(01)	00	11	11
10	01	(10)	01	(10)
11	(11)	01	(11)	01

b) Describe stable and unstable states in a fundamental mode sequential machine. (4M)

(OR)

5. Design a Hazard free OR- AND- network for the Boolean function F= ∑m(0,2,6,7) (10M)

SECTION – III

6. Design a 32 bit carry look ahead adders.(10M)

(OR)

7a) Find a minimum row PLA table to implement the following equations. (6M)

x(A,B,C,D) =∑m(3,6,7,11,15)
y(A,B,C,D) =∑m(1,3,4,7,9,13)
z(A,B,C,D) =∑m(4,6,8,10,11,12,14,15)

b) Implement a full adder using ROM. (4M)

SECTION – IV

8. a) A circuit realizes the function $z = x_1'x_4+x_2'x_3+x_1x_4'$. Using the Boolean difference method, find the test vectors for SA0 faults and SA1 faults on all input lines of the circuit. (6M)

   b) Explain in detail about fault classes and models. (4M)

(OR)

9. Apply Kohavi's algorithm for the given POS function F=(A+B')(C+BD) (10M)

SECTION – V

10. a) Draw the SM chart of binary multiplier. (6M)
    b) Write short notes on equivalent SM blocks.(4M)

(OR)

11. Draw the SM chart of the Dice game controller. (10M)

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MRCET

R15A0507

JAVA PROGRAMMING

Code No: R15A0507

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

Java Programming

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART – A **(25 Marks)**

1. (a) Explain Scope and lifetime of the variables?(2M)
   (b) What is Inner Class? (3M)
   (c) What is an Interface? (2M)
   (d) Explain about Super Keyword? (3M)
   (e) Write the differences between throw and throws keyword? (2M)
   (f) Explain about Daemon threads? (3M)
   (g) What is an Event Listeners? (2M)
   (h) Write the differences between applets and applications? (3M)
   (i) What is an applet? (2M)
   (j) What is the Layout manager? (3M)

PART – B **(50 Marks)**

SECTION – I

2. What is access control? How access control is implemented in java? (10M)

(OR)

3. Explain about String class methods with an example program? (10M)

SECTION – II

4. Explain about runtime polymorphism with an example program? (10M)

(OR)

5. How to access a package and also write the uses of creating a package? (10M)

SECTION – III

6. Explain how to create built in exceptions with example program? (10M)

(OR)

7. Explain about thread life cycle in details.? (10M)

SECTION – IV

8. Write about mouse event handling? (10M)

(OR)

9. Explain about Adapter class with an example program? (10M)

SECTION – V

10. Explain about border Layout? (10M)

(OR)

11. Explain below AWT controls

a)Text Field (3M) b)choice (3M) c)Scrollbar(4M)

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Code No: R15A0507

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations, November 2017

Java Programming

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A (25 Marks)

12. (a) What are OOPS concepts?(3M)
    (b) Explain about Method Overriding? (2M)
    (c) What is an abstract class? (3M)
    (d) Explain about Final Class and Methods? (2M)
    (e) What are checked exceptions? (3M)
    (f) Write about thread priorities? (2M)
    (g) What is Event Source? (3M)
    (h) How to pass parameters to applets? (2M)
    (i) What is Layout manager? (3M)
    (j) Explain about ‘ this’ keyword? (2M)

PART – B (50 Marks)

SECTION – I

13. Explain about Java Buzzwords?

(OR)

14. Explain Constructor Overloading with an example program?

SECTION – II

15. Define Inheritance and explain different types of Inheritances with example programs ?

(OR)

16. Explain steps for creating a package?

SECTION – III

17. Explain Exception handling mechanism in java?

(OR)

18. Explain thread life cycle? How to create threads using thread Class?

SECTION – IV

19. Explain life cycle of an applet?

(OR)

20. Explain file handling mechanism using FileInputStream and FileOutputStream?

SECTION – V

21. Explain about the below AWT controls
    a)Button (3M) b)check box (4M) c)scrollbar (3M)

(OR)

22. Explain the difference between AWT and Swings?

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Java Programming

Model Paper – 1(R15)

III ECE I Semester

Duration: 3hrs **Max Marks: 75**

Answer all the following

PART-A **(Marks 25)**

1. (a) What are the properties of object oriented programming?
   (b) What is method overriding?
   (c)Define an Exception. What is meant by Exception Handling?
   (d)List some of the classes available in collection?
   (e)List the components of Swing?
   (f)Discuss briefly about streams.
   (g)What is inheritance?
   (h)What is thread priority?
   (i)What are the steps involved in creating Thread life Cycle?
   (j)What is an event?

Answer all the questions

PART – B **(Marks: 5*10=50)**

2. (a)Discuss in detail about inheritance. Also write its benefits.

   (OR)

   (b)Describe about Type conversion. Also explain how casting is used to perform type conversion between incompatible types.

3. (a) What is inheritance ? Explain different types of inheritance.

   (OR)

   (b) How a method can be overridden? Explain.

4. (a) Give the class hierarchy in Java related to exception handling. Briefly explain each class.

   (OR)

   (b)What is a thread? Explain the states of a thread with an example.

5. (a) Explain in detail about collection interfaces.

   (OR)

   (b) Explain in details about different Layout Manager

6. (a) Explain in detail about the classification of swing components.

   (OR)

   (b)Explain in brief about events and event sources.

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Java Programming

Model Paper –2 (R15)

III ECE I Semester

Duration: 3hrs **Max Marks: 75**

Answer all the following

PART-A **(Marks 25)**

1. (a) What is Data Abstraction? (2M)
   (b) Compare AWT and Swings? (3M)
   (c) Explain about operators in Java? (2M)
   (d) Explain final keyword with example? (3M)
   (e) Explain about the usage of this keyword with example? (2M)
   (f) Explain inner classes in java? (3M)
   (g) Explain the differences between throw and throws (2M)
   (h) Explain the Array List class? (3M)
   (i) What is Dynamic Binding (2M)
   (j) Difference between Applet and Applications? (3M)

PART – B **(Marks: 5*10=50)**

Answer all the questions

2. (a) What is Parameter Passing? Explain with Program? (5M)
   (b)What is Recursion? Write a program for Factorial of number using Recursion? (5M)

(OR)

(c) Explain about String Buffer class methods in java? Explain about Access Control (5M) 3 (a) Define an interface? Explain about Abstract class with Program? (10M)

(OR)

(b) How multiple inheritances are achieved in java with the interfaces? Explain with an example? (10M)

4 (a) Explain Exception Handling Mechanism in java with programs (10M)

(OR)

(b) What is Inter thread Communication? Explain Producer Consumer pattern with program? (10M)

5 (a) Explain the difference between: i) Hash Table. ii) Vector class (10M)

(OR)

(b)Explain Forms of inheritance in java with examples (10M)

6 (a) Write a java program for Handling Mouse Events and Key Events? (10M) (OR)

(b) Explain about Swing Components: i) JButton ii) JLabel iii) JTextArea iv) JTextField (10M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Java Programming

Model Paper –3 (R15)

III ECE I Semester

Duration: 3hrs **Max Marks: 75**

Answer all the following

PART-A **(Marks 25)**

1. (a) List the data types present in java.
(b)Explain in brief about interfaces.
(c)What is meant by checked exception and unchecked exception.
(d)How statements call can be used? Also list the types of methods in statement class.
(e)Discuss about JFrame and JPanel
(f)Discuss briefly about enumerated data types.
(g)What is CLASSPATH ?
(h)What is multithreading?
(i) Explain Enumeration and Autoboxing
(j)What are event sources?

PART – B **(Marks:5*10=50)**

Answer all the questions

1. (a)List the primitive data types of java. Explain each of them in detail.

(OR)

(b)What are the different types of array? List out the advantages of using arrays?

2. (a)Write in detail about super class and subclasses.

(OR)

(b)Write the differences between interfaces and abstract.

3. (a)How are finally statements used in java? Explain in detail.

(OR)

(b)Is it possible to interrupt a thread? Explain.

4. (a) Explain in detail about hash table class.

(OR)

(b) Explain about Forms of Inheritance in Java with examples.

5. (a) Discuss in detail about swing components.

(OR)

(b)Explain about various event classes and Event Listeners

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Java Programming

Model Paper –4 (R15)

III ECE I Semester

Duration: 3hrs **Max Marks: 75**

Answer all the following

PART-A **(Marks 25)**

1. (a) What are the OOPs features? (2M)
   (b) Compare Procedural and OOP Languages? (3M)
   (c) Explain about control statements in java? (2M)
   (d) Explain about method overloading with example? (3M)
   (e) Explain about the usage of super keyword with an example? (2M)
   (f) Explain how interfaces are implemented with an example? (3M)
   (g) Explain the following: try, catch, throw, throws, finally (2M)
   (h) Explain the creation of threads with an example? (3M)
   (i)List Event classes in java(2M)
   (j)What are event sources and explain the life cycle of an applet? (3M)

PART – B **(Marks: 5*10=50)**

Answer all the questions

2. (a)What is type casting and conversion? When it is required? (5M)
   (b)What is an array? How arrays are declared in java with an example? (5M)

(OR)

(c) Explain about method overloading with example? Explain about constructor overloading with example? 3
(a) What is method overriding? How method overriding is achieved in Java, with an example? (10M)

(OR)

(b) How multiple inheritances are achieved in java with the interfaces? Explain with an example? (10M)

4 (a) What are the checked Exceptions and Unchecked Exceptions? Explain some of these exceptions with an example and also give the difference between them. (10M)

(OR)

(b) How the priorities can be assigned to threads? Explain with example? (10M)

5 (a) Explain the difference between: i) Vector and Array List. ii) Enumeration and Iterator. (10M)

(OR)

(b)Explain in detail about MVC Architecture and Explain about Adapter classes(10M)

6 (a) Define an event. Give examples of events. Define event handler. How it handles events? (10M)

(OR)

(b) Explain about layout manager? With an example? (10M)

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Java Programming

Model Paper –5 (R15)

III ECE I Semester

Duration: 3hrs **Max Marks: 75**

Answer all the following

PART-A (Marks:25)

1. (a) What is Polymorphism? (2M)
   (b) Compare Class and Interface with examples? (3M)
   (c) Explain about Access Control in java? (2M)
   (d) Explain Generics in java? (3M)
   (e) Explain about the usage of this keyword with example? (2M)
   (f) Explain java Buzzwords? (3M)
   (g) Explain Garbage Collection (2M)
   (h) Explain the Vector class? (3M)
   (i) What is Static Binding (2M)
   (j) Explain how to pass parameters to an applet? (3M)

PART – B (Marks: 5*10=50)

Answer all the questions

2. (a) What is Type Casting ? Explain Type Conversion in Java with example? (5M) (b)Explain Constructor Overloading and Method Overloading with program? (5M)

(OR)

(c) Explain about String class methods in java? (5M)

3 (a) Define an interface? Explain how to implement an interface with program? (10M) (OR)

(b) What is a Package? Explain how to create User defined package with program (10M)

4 (a) Explain Exception Handling Mechanism in java with programs (10M)

(OR)

(b) What is Inter thread Communication? Explain Producer Consumer pattern with program? (10M)

5 (a) Explain about MVC Architecture? Explain AWT Components like Label, Button, Checkbox (10M) (OR)

(b)Explain Forms of inheritance in java with examples (10M)

6 (a) Explain different Layout Managers in java (OR)

(b) Explain about Swing Components: i) Combo boxes ii) Tabbed Panes iii) Tables iv) Trees (10M)

PREVIOUS QUESTION PAPERS

R15

Code No: R15A0507

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech II Semester Regular Examinations, April/May 2017

Java Programming

(CSE)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART – A (25 Marks)

1. (a) Discuss OOPs concepts. (3)
   (b) Compare method and a constructor.(3)
   (c) What are the uses of super keyword. (2)
   (d) What is an interface. (2)
   (e) Discuss the significance of finally block (2)
   (f) Illustrate with a neat diagram thread life cycle. (3)
   (g) Explain hashtable with an example. (3)
   (h) Discuss the four driver types needed for JDBC connectivity. (3)
   (i) Differentiate an applet and an application. (2)
   (j) What is event delegation model. (2)

PART – B (50 Marks)

SECTION – I

2. a) Illustrate with an example parameter passing in Java. (5)
   b) Demonstrate the use of this keyword with an example. (5)

(OR)

3. a) Discuss method overloading with an example. (5)
   b) Illustrate the various functions of String class with an example. (5)

SECTION – II

4. a) Show how multiple inheritance is achieved in Java with an example. (5)
   b) Explain with an example the need of inner classes. (5)

(OR)

5. a) Discuss dynamic method dispatch with an example. (5)
   b) Write the steps in defining, creating and accessing a package. (5)

SECTION – III

6. a) Explain throws statement in Java with an example. (5)
   b) Why thread is called lightweight and process heavy weight task. (5)

(OR)

7. a) Demonstrate nested try blocks with a suitable example. (5)
   b) How to create multiple threads in Java with a suitable example. (5)

SECTION – IV

8. a) Compare Array List with Hash table. (5)
   b) Demonstrate FileOutputStream with an example. (5)

(OR)

9. a) Explain updating data with JDBC. (5)
   b) Illustrate RandomAccessFile operations with suitable examples. (5)

SECTION – V

10. a) Discuss any two swing applications. (5)
    b) Illustrate with a neat diagram applet lifecycle. (5)

(OR)

11. a) Write a program for handling mouse events. (5)
    b) Write a program to illustrate border and grid layout managers (5)

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Code No: R15A0507

R15

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

II B.Tech I Semester supplementary Examinations, May 2017

Java Programming

(ME)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART - A (25 Marks)

1.(a)Explain the benefits of OOP? [2M]
(b) What is instance? How it is different from class? [3M]
(c) Define package. [2M]
(d) What is polymorphism? [3M]
(e) What is an Exception? [2M]
(f) Write the difference between thread and process? [3M]
(g) What is JDBC? [2M]
(h) What is the difference between List and Set? [3M]
(i) Explain the advantages of Swings. [2M]
(j) Explain the different types of applets. [3M]

PART - B (50 Marks)

SECTION - I

2.a) Explain about String and String Buffer classes.
b) What is constructor? Explain different types of constructors in Java.

OR

3. Explain b*riefly about Java Buzzwords?*.

SECTION – II

4. Explain different types of Inheritance with suitable examples.

OR

5. What is a Package? Explain the procedure for creating and importing the Packages in java.

SECTION – III

6. What is exception? Explain the exception handling mechanism.

OR

7. Explain about thread synchronization.

SECTION – IV

8. a) What are the main steps in java to make JDBC connectivity?
b) Give the list of important Interfaces of Collection API.

OR

9. a).Explain the commonly used methods of Input Stream class.
b) Explain different types of database drivers.

SECTION – V

10.a) What is an event? Explain the event delegation model.
b) Write a java program to handle keyboard events

OR

11. a). Write the HTML Applet Tag and explain each part of it.
b) What is the lifecycle of an applet?

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R15

Code No: R15A0507-161

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

B.Tech. III Semester Regular Examinations, NOV 2016

JAVA PROGRAMMING

(ME)

Roll No			N	3						

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B
Part A is compulsory which carriers 25 marks and Answer all questions.
Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

PART - A (25 Marks)

1..(a) What is type casting? [2M]
(b) Define class and object [3M]
(c) Explain abstract classes [2M]
(d) Explain Method overloading [3M]
(e)What is an interface? [2M]
(f)What is synchronization? [3M]
(g) What is CLASSPATH? [2M]
(h) Write a java code to print date and time. [3M]
(i) Give the benefits of exception handling. [2M]
(j)write a short note on inner classes. [3M]

PART - B (50 Marks)

SECTION - I

2.a) What is recursion ?write a recursive function for factorial?
b) Explain about different parameter passing methods with examples.

OR

3. a)Write a java program to find the sum of all elements in the one dimensional array.
b) What is Overloading? Explain Method overloading with an example.

SECTION – II

4. (a) Explain the member access mechanism in inheritance with an example.
(b) What is polymorphism? Write a program to find the perimeter of the triangle and circle

OR

5. (a) What is multiple inheritance? Explain how it can be implemented in Java with the help of an example.
(b) Compare and contrast overloading and overriding methods.

SECTION – III

6.(a)Distinguish between multi threading and multi tasking.
(b) Explain about the keywords try, catch, throw and throws.

OR

7. (a)Explain the thread Life cycle.
(b)Explain various checked and unchecked built-in Exceptions.

SECTION – IV

8. a) Explain File Input Stream and File Output put Stream with an example for each.
b) Explain briefly various legacy classes and interfaces in java.util package.

OR

9. Explain scanner class and StringTokenizer class with an example

SECTION – V

10. a) Write an applet to create registration form of a student.
    b) Explain border and grid layout mangers briefly.

OR

11. a). What are the differences between applications and applets?
    b) Explain AWT controls in briefly.

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R15

Code No: **R15A0569**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations, May 2018

Computer Organization & Operating systems

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B

Part A is compulsory which carriers 25 marks and Answer all questions.

Part B Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 10 marks.

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PART – A (25 Marks)

1. (a) Discuss about floating point representation. (2M)
   (b) Find (1001101 - 10101001) using 1's complement? (3M)
   (c) Draw the block diagram of associative memory. (2M)
   (d) Discuss microoperation and microinstruction. (3M)
   (e) Discuss destination initiated transfer using handshaking. (2M)
   (f) Write the three ways computer buses can be used to communicate with memory and I/O. (3M)
   (g) What are the necessary conditions for the occurrence of deadlock? (2M)
   (h) What is demand paging? (3M)
   (i) Explain the bit vector representation of free space management. (2M)
   (j) List the four approaches to free –space management. (3M)

PART – B (50 Marks)

SECTION – I

2. a) Explain the following with neat sketches:
   i) 4 – bit Binary adder ii) Binary Adder – Subtractor (5M)
   b) Explain how registers are connected to common bus in the computer with a neat diagram. (5M)

(OR)

3. a) Explain 4-bit binary incrementer with a neat diagram (5M)
   b) Find 2's complement of the following (5M)
   (i) 10010 ii) 111000 iii) 0101010 iv) 111111

SECTION – II

4. Discuss the design of control unit. (10M)

(OR)

5. Discuss the memory mapping functions to place memory blocks in the cache. (10M)

SECTION – III

6. a)Why does DMA have priority over the CPU When both request a memory transfer? (5M)
   b) Discuss asynchronous data transfer. (5M)

(OR)

7. What is the difference between isolated IO and memory mapped I/O? State the advantages and disadvantages of each. (10M)

SECTION – IV

8. a) Write about deadlock conditions and bankers algorithm in detail. (5M)
   b) What is a page fault? Explain the steps involved in handling a page fault with a neat sketch. (5M)

(OR)

9. a) How does deadlock avoidance differ from deadlock prevention? Write about deadlock avoidance algorithm in detail. (5M)
   b) What are the disadvantages of single contiguous memory allocation? Explain. (5M)

SECTION – V

10. a) Explain directory implementation. (5M)
    b) Discuss contiguous allocation of disk space. (5M)

(OR)

11. a) Explain a typical file control block. (5M)
    b) Illustrate and discuss linked allocation of disk space with a neat diagram. (5M)

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